PLECS REAL-TIME SEMINAR

Code Generation and Hardware-In-the-Loop Testing with PLECS Friday, March 17, 2017 at North Carolina State University in Raleigh

Speakers	Dr. Beat Arnet, General Manager, Plexim
	Ms. Manaswini Parimi, Applications Engineer, Plexim
8:30am	Setup, networking, coffee and muffins (provided)
9:00am	Introduction to general use of PLECS Blockset and PLECS Standalone I Fast and efficient semiconductor models with instantaneous switching I Variable and fixed-step operation I Electrical, thermal, magnetic, mechanical and control components Hands-on exercises: I Buck converter I Modeling and measuring thermal loss
	Designing an inductor in the magnetic domain
10:30am	Coffee break (provided)
10:45am	PLECS Solver and Coder ►I Definition of stiff and non-stiff systems ►I Explicit and non-explicit solvers ►I Coder options and code generation ►I CodeGen simulation mode
	Hands-on exercises: ►I Solver accuracy and settings ►I Code generation with generic target
12noon	Lunch (provided)
1:00pm	Introduction to Hardware-In-the-Loop and PLECS RT Box I Overview of different "in-the-loop" methodologies I Using the RT Box for HIL I RT Box architecture and specifications I IO processing Hands-on exercises:
	 Discretization of Buck converter Ideal and averaged switch models
3:00pm	Coffee break (provided)
3:15pm	 RT Box demos and discussion ▶I Buck/boost converter at 20 kHz switching ▶I Field oriented control of PM motor with quadrature encoder ▶I 3-level NPC grid-tied solar inverter
5:00pm	End of seminar
Contact	RSVP to Ms. Manu Parimi, parimil@plexim.com, 617-209-2126 (include any special dietary needs)

+1 617 209 2121 info@plexim.com www.plexim.com

