



## **PLECS Workshop**

Tallinn University of Technology, Energy Building (NRG), Ehitajate tee 5, Tallinn, Estonia

13.01.2026, TalTech, NRG-223 Advanced Modeling and Simulation of Power Electronic Systems		
10:00	Introduction to PLECS	
	<ul> <li>General use of PLECS Blockset and PLECS Standalone</li> </ul>	
	<ul> <li>Instantaneous switching</li> </ul>	
	Variable and fixed-step operation	
	Exercise: Modeling a switched-mode power supply!	
11:30	Break	
12:00	Solver Settings	
	Definition of stiff and non-stiff systems	
	Explicit and non-explicit solvers	
	Stability domains	
	Accuracy considerations, step size control	
	<ul> <li>Proper handling of discontinuities, zero-crossing detection</li> </ul>	
13:00	Lunch	
14:00	Introduction to Thermal Simulation	
	<ul> <li>Switching &amp; conduction loss descriptions</li> </ul>	
	Combined electrical-thermal simulation	
	<ul> <li>Determining loss values from data sheets</li> </ul>	
	Exercise: Thermal modeling of a buck converter!	
15:30	Break	
16:00	Bringing Simulation and Real Hardware Together	
	(Code Generation Workflow in PLECS)	
	Automatic code generation for microcontrollers	
	Plant code generation for the RT Box	
	<ul> <li>Nanostep®, FlexArray and CPU solver engines</li> </ul>	
	<ul> <li>Real-time simulation with 4ns step size for MHz switching</li> </ul>	
	Demonstration: HIL testbench with microcontroller and RT Box	
17:00	Q&A	
17:15	End of Day	

14.01.2026, TalTech, NRG-223		
Real-Time Simulation Using the PLECS RT Box		
09:30	Registration and Installation of Necessary Features	
10:00	Overview and Introduction to RT Box Workflow using PLECS	
	PLECS overview!	
	From PLECS offline models to RCP and HIL!	
	Code Generation!	
10:45	RT Box Introductory Exercise	
	PLECS RT Box features	
	Exercise: Introductory exercise using I/O ports	
11:30	RT Box Library Overview	
11:45	Break	
12:00	Real-time Simulation of a Voltage Source Inverter (VSI)	
	<ul> <li>PLECS model creation using the target blocks library</li> </ul>	
	Deployment on the RT Box	
	Exercise: Voltage Source Inverter (VSI)	
13:00	Lunch	
14:00	Solver Engine	
	RT Box architecture	
	Sub-cycle averaging concept	
	FPGA simulation using FlexArray solver	
	<ul> <li>FPGA simulation using Nanostep® solver</li> </ul>	
	Exercise: Solver engine	
16:00	Break	
16:15	Solver Engine	
	Exercise: Solver engine	
17:00	RT Box Hardware-in-the-Loop (HIL) Application Demo, Q&A	
17:30	End of Workshop	