PLECS WORKSHOP

PIL / HIL Simulation and Advanced Modeling of Power Electronic Systems
Warsaw University of Technology, February 1, 2017

08:30	Registration
09:00	C-Code Integration ▶I Solver operation ▶I Sample time settings ▶I DLL Block Exercise: Efficient PWM generation using the PLECS C-Script block
10:15	Break
10:30	C-Code Integration (Continuation) ▶I Solver operation ▶I Sample time settings ▶I DLL Block Exercise: Efficient PWM generation using the PLECS C-Script block
12:00	Lunch
13:00	Analysis Tools (Multitone Analysis) ▶I Steady state analysis ▶I AC sweep and impulse response analysis
14:00	Principle of a Processor-in-the-Loop Simulation ▶I Integration of PIL ▶I Integration of the PIL framework into an embedded project ▶I Setting up PLECS for PIL
15:00	Break
15:15	Hardware-in-the-Loop (HIL) Simulation using the PLECS RT Box ▶I Basic hardware structure ▶I Difference between models in HIL and offline-simulation ▶I Technologies for large scale models in HIL ▶I Demo of different power electronic systems
16:00	What's New in PLECS / Q&A
16:30	End of Workshop
Contact	Plexim GmbH, +41 44 533 51 00, info@plexim.com
Location	Warsaw University of Technology, Main Building (Gmach Główny), Room 443, Pl. Politechniki 1, 00-661 Warszawa, Poland
Note	This workshop addresses to anyone who already has experience with the simulation software PLECS.

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