

PLECS WORKSHOP

Processor-in-the-Loop Simulation and Advanced Modeling of Power Electronic Systems Day 2
Fraunhofer ISE Freiburg, January 28th, 2015

08:30	Registration
09:00	Analysis Tools (New Multitone Analysis) <ul style="list-style-type: none">▶ Steady state analysis▶ AC sweep and impulse response analysis Exercise: Control design of a flyback converter using PLECS
10:15	Break
10:30	Principle of a Processor-in-the-Loop simulation <ul style="list-style-type: none">▶ Integration of PIL▶ Framework into an embedded project▶ Setting up PLECS for PIL Exercise: PIL simulation for a BLDC motor control
12:00	Lunch
13:00	Processor-in-the-Loop simulation (continuation) Exercise: PIL simulation for a BLDC motor control
14:00	Break
	Code Integration via C-Script and DLL block <ul style="list-style-type: none">▶ Solver operation▶ Sample time settings▶ DLL block Exercise: Efficient PWM generation using the PLECS C-Script block Q&A
17:00	End of day
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