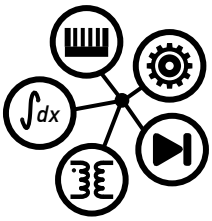

PLECS

DEMO MODEL

Series Capacitor Buck Converter

Last updated in PLECS 4.3.1

1 Overview

This demonstration shows a two-phase series capacitor buck converter circuit with constant on-time control as proposed in [1].

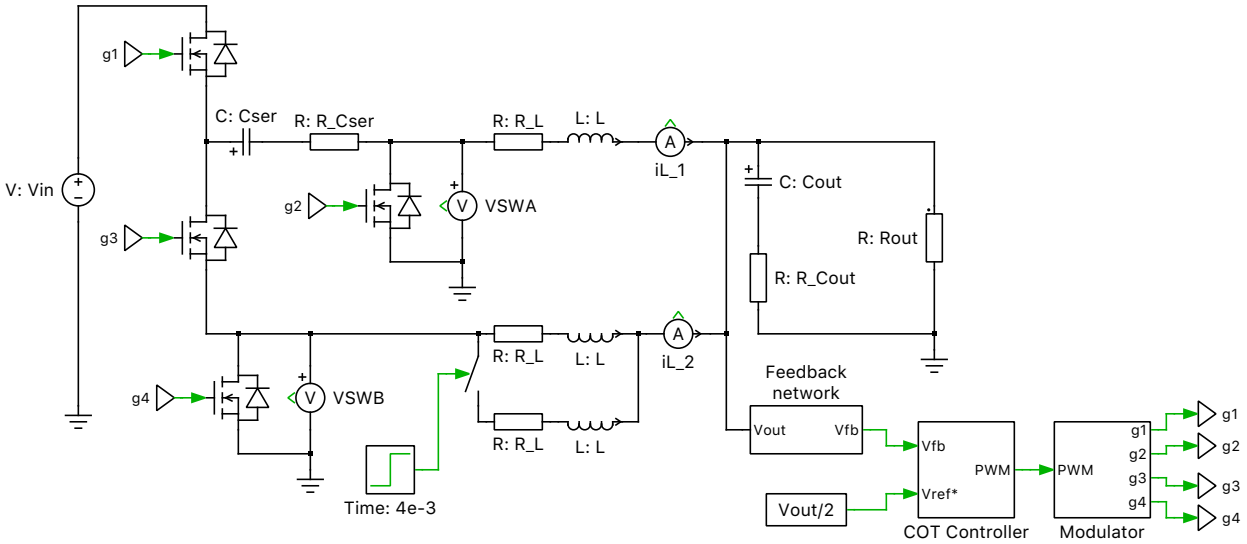

Figure 1: Two-phase series capacitor buck converter circuit with constant on-time control

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Note This model contains model initialization commands that are accessible from:

PLECS Standalone: The menu **Simulation + Simulation Parameters... + Initializations**

PLECS Blockset: Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

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2 Model

2.1 Power circuit

The series capacitor buck converter is a DC/DC topology combining a switched capacitor circuit and a two-phase buck converter into a single-stage. The series capacitor (whose voltage is half the input voltage nominally) provides a 2-to-1 voltage step-down. From the perspective of the output filter, it looks like a buck converter with half the input voltage. The switch nodes (VSWA and VSWB) see only half the input voltage instead of the full input voltage in a buck converter, reducing the switching loss.

This topology automatically balances inductor currents without any current sensing circuits or load-sharing control loops. The converter has a 50 percent duty-cycle limitation, which combined with the inherent 2-to-1 voltage step-down created by the series capacitor, dictates the maximum possible output voltage to be one-fourth the input voltage. The practical limit of the output voltage may be one-fifth the input voltage [1]. In the current demo, the desired output voltage is one-tenth the input voltage.

2.2 Control

The output voltage of the circuit is regulated by using constant on-time control. This is a variable frequency solution where the on-time is held constant. The control uses the output voltage ripple (V_{fb}) as

a PWM ramp signal. This signal is compared to the reference ($V_{\mathrm{ref}*}$), therefore, some output voltage ripple is required. This is provided by the output capacitor ESR. The comparator monitors the feedback voltage (V_{fb}) and triggers a high side switch on-time when the feedback output is lower than the reference value. The controller only modulates the switch-off time, since the on-time is held constant. Additionally, a Minimum Off-time block prevents inductor saturation during a rapid change of load. Constant on-time control is particularly beneficial for large voltage step-downs (low duty cycle) [3].

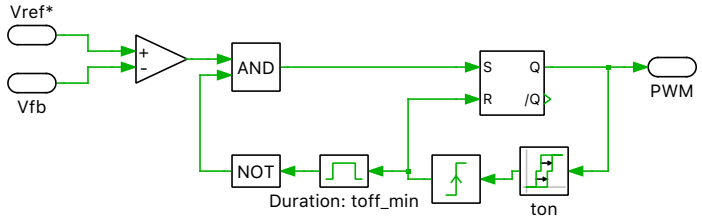

Figure 2: Controller schematic

3 Simulation

Run the simulation to observe the steady-state operation of the converter for a 12 V input point of load (POL) voltage-regulator application. The average series capacitor voltage is approximately half the input voltage (6 V), the load voltage is approximately one-tenth the input voltage (1.2 V) and both the switch node voltages, VSWA and VSWB, are limited to half the input voltage (6 V). Additionally, the inductor currents are perfectly balanced.

Automatic inductor current balancing can be demonstrated by varying the value of one of the inductors. At the start of the simulation, both the inductors are set to 220 nH. At t = 4 ms, inductance of one of the phases is changed to 110 nH. The simulation results Fig. 4 show that the average inductor currents (i_{L1} green i_{L2} red) continue to be balanced and provide the same current to the output.

References

[1] Pradeep Shenoy, “Design of a high-frequency series capacitor buck converter,” white paper from the TI Power Supply Design Seminar 2016/17.

[2] Pradeep Shenoy, “Introduction to the Series Capacitor Buck Converter.”
Click to access online: Texas Instruments SLVA750A Application Report.

[3] Robert Mammano, “Switching control algorithms,” in Fundamentals of Power Supply Design, 1st ed.

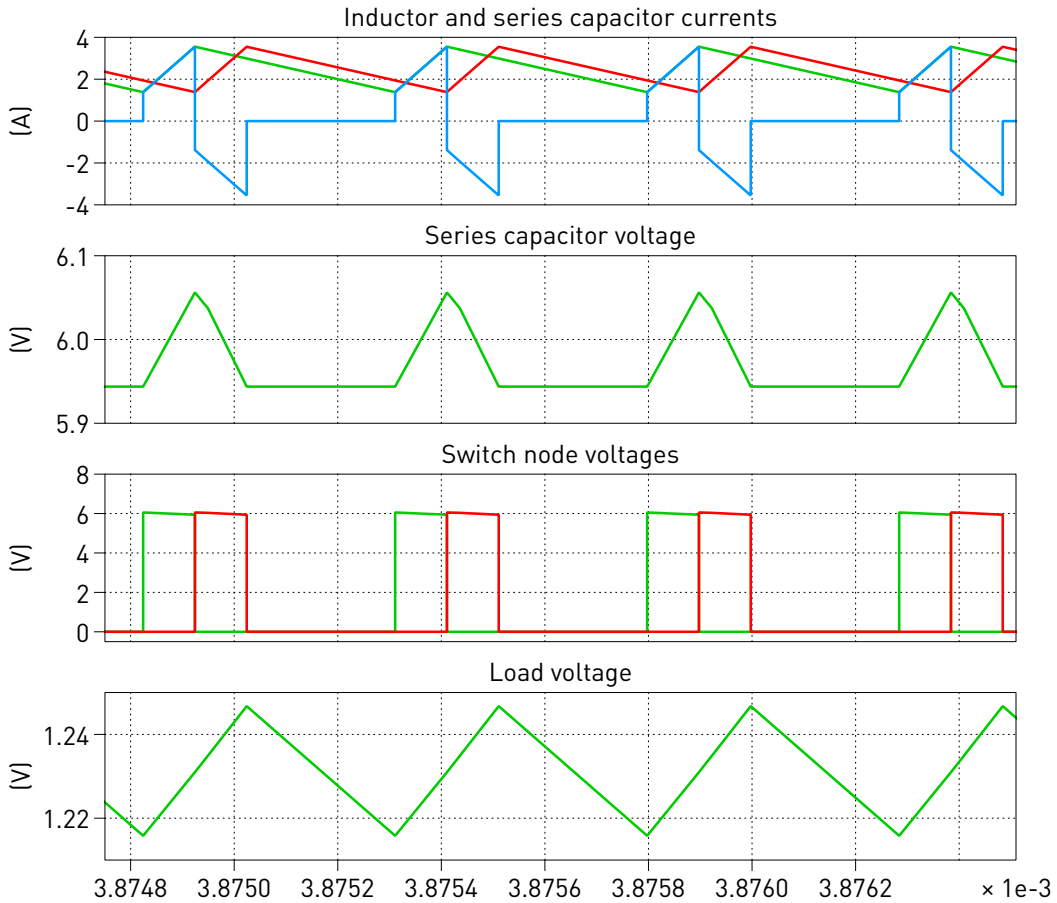

Figure 3: Simulation result in steady-state operation

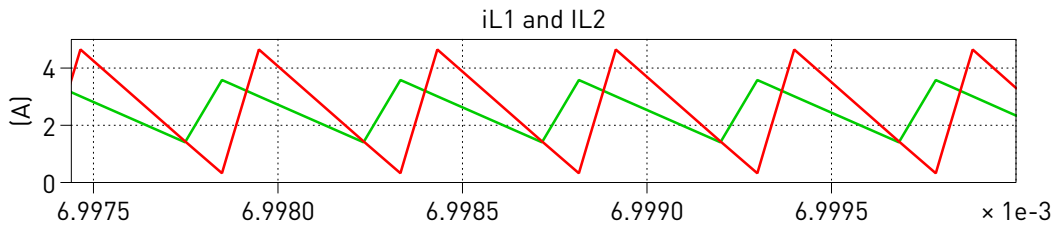

Figure 4: Average inductor currents

Revision History:

PLECS 4.3.1	First release

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PLECS Demo Model