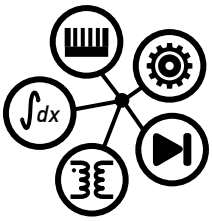

PLECS

DEMO MODEL

Synchronous Buck Converter

Last updated in PLECS 4.4.2

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1 Overview

This demonstration shows a regulated synchronous buck converter with a fixed load and switched load in parallel.

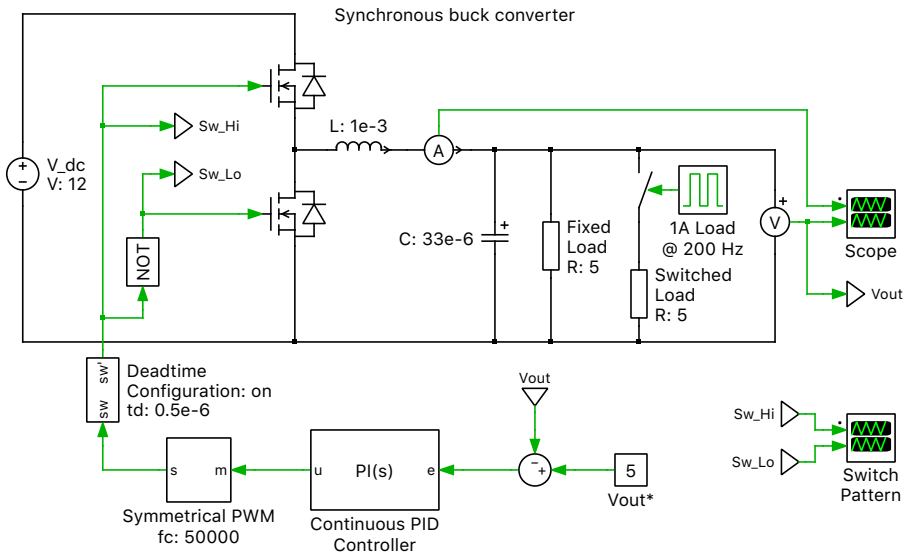

Figure 1: Synchronous buck converter

2 Model

2.1 Power circuit

A synchronous buck converter topology is used to step down a 12 VDC input to produce 5 VDC at the output. The load consists of a 5 Ω fixed resistive load as well as a 5 Ω pulsed resistive load that cycles at 200 Hz. In a synchronous buck converter the freewheeling diode is augmented by an active switch, which has the advantage of improved converter efficiency in practice, although on-resistance of the MOSFETs and thermal loss modeling have not been included in this example. As compared to a traditional buck converter, a synchronous buck converter always operates in continuous conduction mode (CCM) since current can reverse in the second MOSFET.

2.2 Control

The switch modulation is generated by a Symmetrical PWM component, where the modulation index is provided via feedback control. The output voltage is measured and compared with a 5 VDC setpoint. The generated voltage error is passed through a PI controller to determine the duty cycle of the FETs. The duty cycle range is limited between 1% and 99%, and thus a loop is used to prevent wind-up of the integrator. The two switches are then modulated in a complementary manner. In practice, it is important not to gate both switches on at the same time to avoid shoot-through. This is prevented by introducing a dead time to delay the turn-on of the opposing switches. For more details on designing regulators using PLECS, please see the demo model “Power Supply Compensator Analysis” in the PLECS demo models library.

3 Simulation

The simulation result shown in Fig. 2 demonstrates the start-up of the converter and two load current steps. During each load current change the perturbation in the output voltage and the response of the regulator can be observed. This model can be used as a starting point to explore both the electronics and regulator for practical designs.

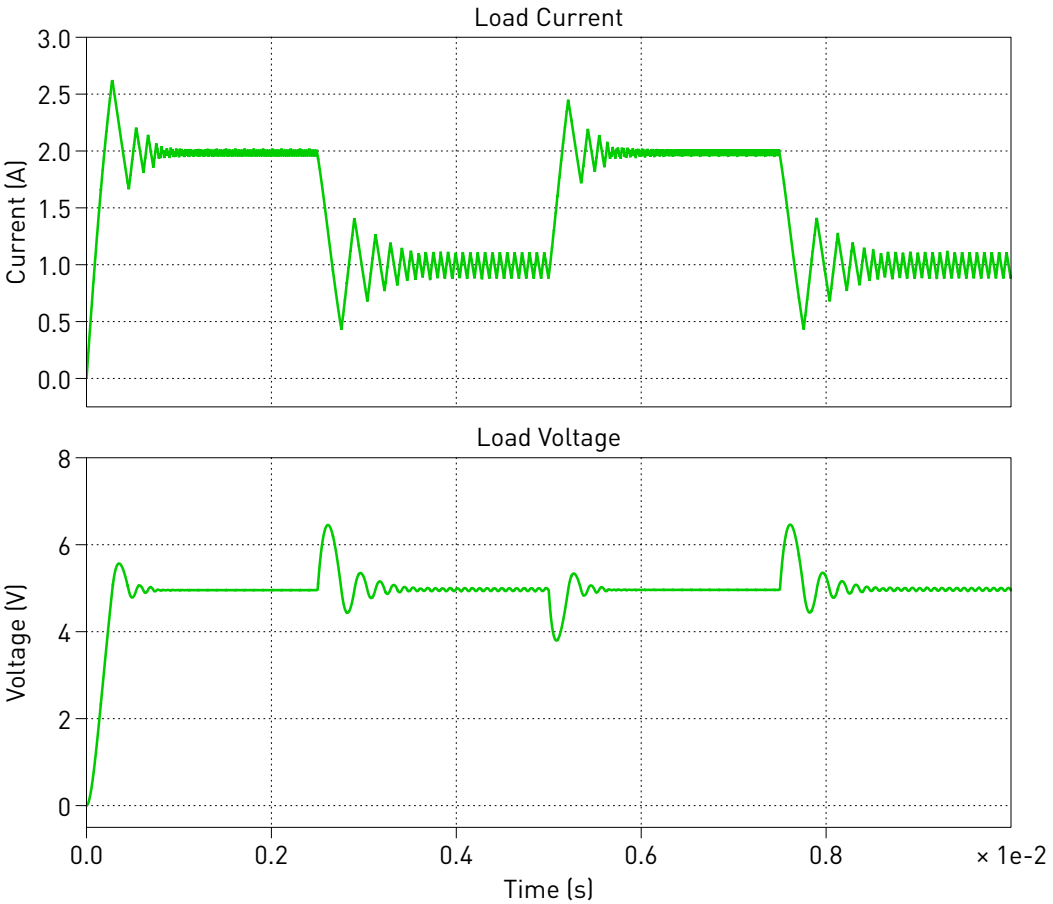

Figure 2: Simulation result of synchronous buck converter in closed loop under load step

Revision History:

PLECS 4.3.1	First release
PLECS 4.4.2	Update PI controller component

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PLECS Demo Model

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