



PLECS

DEMO MODEL

Flying Capacitor Single-Phase Inverter

Last updated in PLECS 4.3.1

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1 Overview

This model shows a flying capacitor (FC) single-phase full bridge voltage source inverter (VSI). The FC VSI is a type of multilevel inverter that can produce a staircase AC waveform of magnitude $V_{dc}/2$ by stacking switching cells to form an inverter leg. When arranged in a full bridge manner, as shown here, the inverter produces $+V_{dc}/-V_{dc}$ across the RL load. This model builds off of the demo model “Flying Capacitor DC-DC Converter” in the PLECS demo models library.

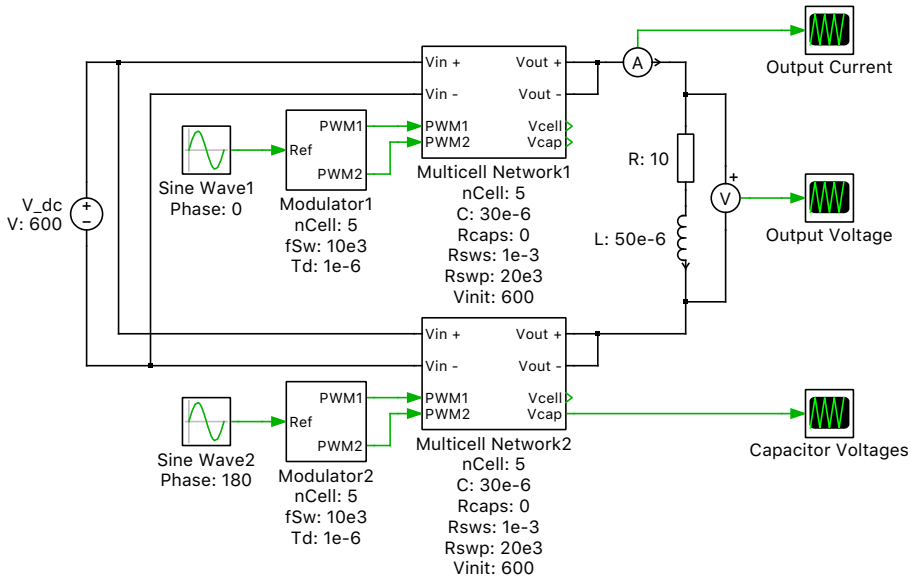


Figure 1: Flying capacitor single-phase inverter

2 Model

2.1 Power circuit

The circuit is modeled as a modular multilevel VSI, where the two switches in each switch pair are connected by a capacitor. The switch pair and capacitors are then connected in series to form a chop-per circuit network. A DC voltage source is connected at the input, and the output of the switch capacitor network is an AC quantity. The generic configurable-length multicell network is shown in the figure below. The generic configurable-length multicell network is shown in Fig. 2.

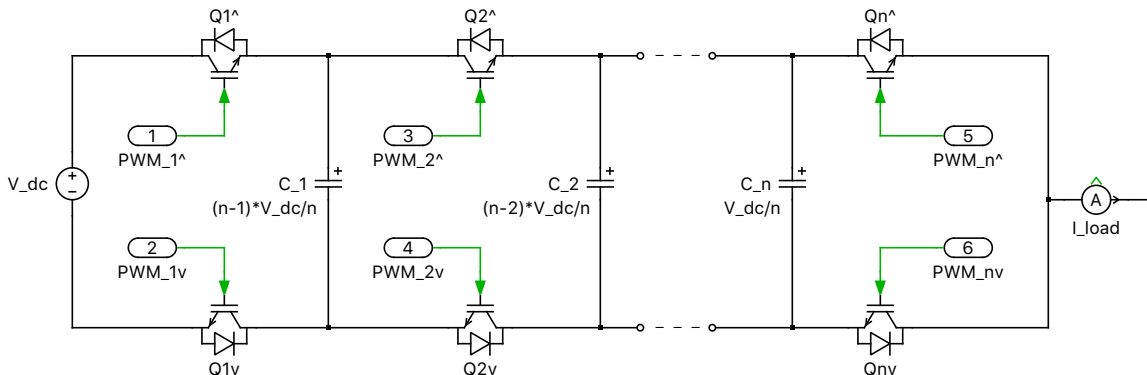


Figure 2: Configurable-length multicell network

The multicell network has been implemented in PLECS using a modular subsystem concept, where a dynamically-sized chain of components is connected using wires and multiplexers. This cell implementation is depicted in Fig. 3. The input and output of the subsystem are configured as the terminals of the flying capacitor chain. The commutation cell is repeated by means of routing its output back into its input $n - 1$ times, for a user-specified number of cells n . As shown below, the trick to this implementation is defining one of the wires in each multiplexer to have a width of $n - 1$. By using a wired loop, this creates a chain with the components in between the multiplexers (a switch pair and clamping capacitor) being replicated in a series-connected fashion n times.

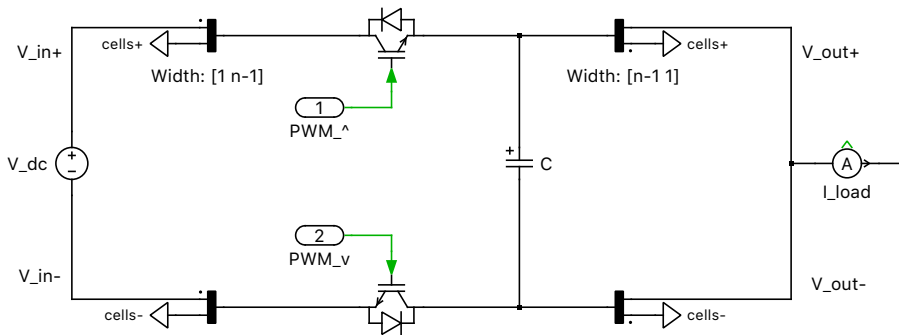


Figure 3: Cell implementation of flying capacitor DC/DC converter

The balanced chopped capacitor voltage levels are $0, V_{dc}/n, 2V_{dc}/n, \dots, (n-1)V_{dc}/n$.

Since the input is 600 VDC and $n = 5$, the capacitor voltage levels are 0, 120, 240, 360, and 480 VDC. The multilevel output voltage waveform is applied to an RL load.

2.2 Control

The modulation scheme is a phase shifted carrier pulse-width modulation (PSCPWM) technique consisting of n triangular carriers, each shifted from the previous one by $2\pi/n$. Sinusoidal reference waveforms are fed into the two modulators, where the reference for the second phase leg has a 180° phase shift compared to the first. The controller provides two pulse-width modulated signals that gate the upper and lower IGBTs with the same duty cycle, but shifted by 180° . A dead time is included to delay the turn-on between switch commutation for each switch pair. The converter doesn't require closed-loop control because the capacitors themselves will self-balance as each commutation cell has equal duty cycles and $2\pi/n$ phase shifts, as discussed in [1] and [2]. Any changes to the DC input will produce a transient, but the system will settle to a well-defined steady-state operating point without feedback regulation.

3 Simulation

Run the simulation with the model as provided to view the signals and verify that the load voltage is a stepped waveform of ± 600 VAC. The result is depicted in Fig. 4. Observe that the capacitor voltages are stacked DC levels of V_{dc}/n . Changing the initial capacitor voltages and rerunning the simulation will show the self-balancing nature of the topology and the capacitor voltages will migrate to their balanced state. Also, the number of cells in the network can be changed, but be sure to set the same number for this parameter in both of the two circuit subsystems and two controller subsystems.

References

- [1] T. A. Meynard, H. Foch, P. Thomas, et al, "Multicell converters: Basic concepts and industry applications", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 955-964, Oct. 2002.

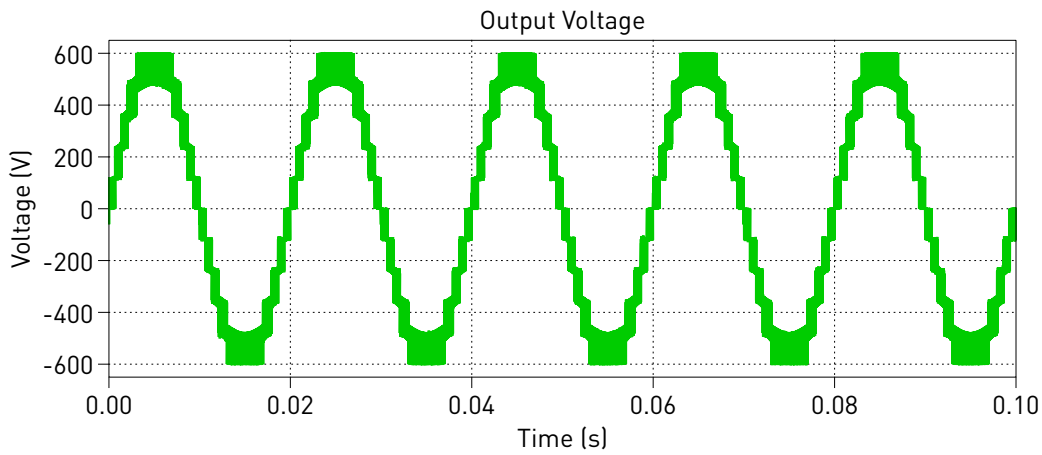


Figure 4: Simulation result of load voltage

- [2] R. H. Wilkinson, T. A. Meynard, and H. du T. Mouton, "Natural balance of multicell converters: The general case", *IEEE Transactions on Power Electronics*, vol. 21, pp. 1658-1666, Nov. 2006.

Revision History:

PLECS 4.3.1 First release

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