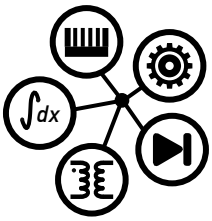

PLECS

DEMO MODEL

Swiss Rectifier with Digital Controller

Last updated in PLECS 4.4.2

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1 Overview

This demonstration shows a Swiss Rectifier (SR) with an output power of $5\,\mathrm{kW}$. The simulation combines the electrical power circuit with digital voltage and current controls.

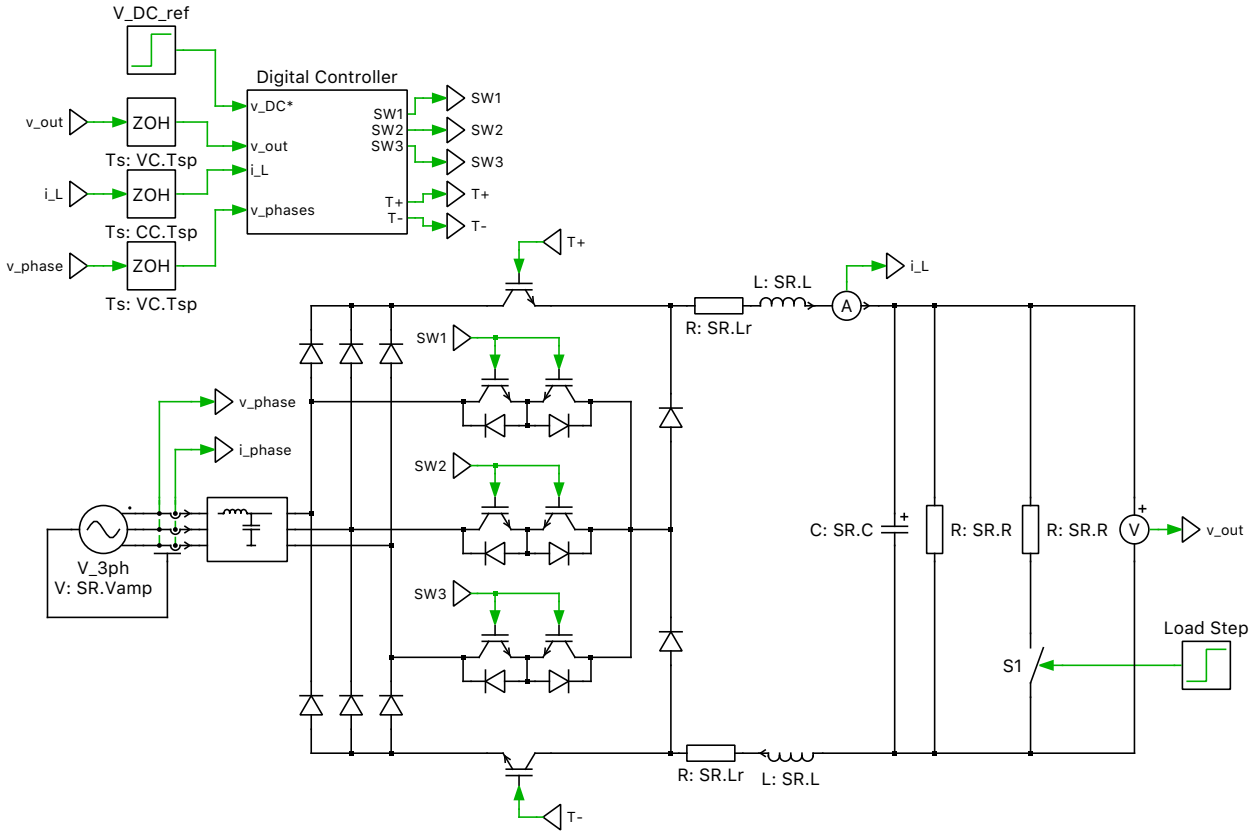

Figure 1: Swiss rectifier

Note This model contains model initialization commands that are accessible from:
PLECS Standalone: The menu **Simulation + Simulation Parameters... + Initializations**
PLECS Blockset: Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

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2 Model

The SR is a unidirectional, three-phase, buck-type, AC-DC converter with power factor correction. The SR consists of a three-phase diode bridge rectifier with two fast switches (T_+ and T_-) on the DC-side of the rectifier. In a normal diode bridge rectifier, only two of the phases carry current over a 60 degree interval. In the SR, a common-emitter based IGBT configuration (SW1 - SW3) is used to implement an injection network. The injection network is switched at twice the line frequency such that current may be injected into the inactive phase by controlling the fast switches. Additionally, an LC input filter is provided to filter the high frequency current harmonics to reduce the harmonic pollution of the grid currents.

2.1 Control

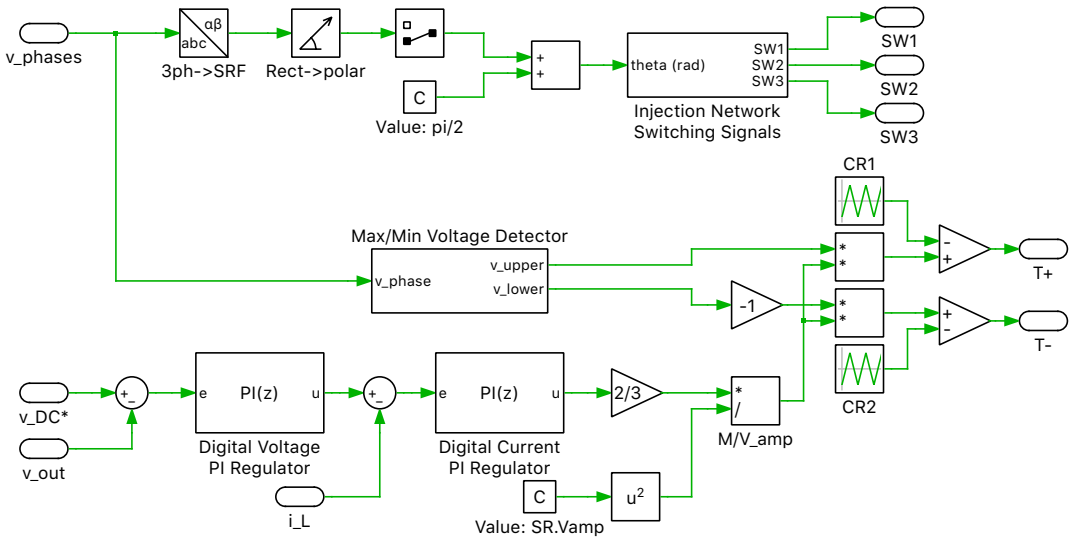

Figure 2: Controller subsystem

The controls of the SR are divided into two main parts: injection-network control and fast-switching controls.

The grid-side three-phase voltages are measured and the instantaneous phase angle is determined. The phase angle information is fed into a look-up table, which is used to generate the switching signal for the injection network switches.

The fast switches of the SR are controlled using a cascaded digital controller with an inner current loop and an outer voltage loop. The output voltage of the SR is measured and compared with a reference. The voltage error is fed into a digital voltage PI regulator and generates a current setpoint. The inductor current is measured and compared with the current setpoint. The error is fed into a digital current PI regulator, which generates a voltage setpoint. This voltage setpoint is translated into a modulation index (M) given by:

$$M = \frac{2 \cdot V_{\text{set}}}{3 \cdot V_{\text{amp}}} \tag{1}$$

where V_{set} is the voltage setpoint generated by the current regulator and V_{amp} is the peak value of the three-phase grid voltage.

The three-phase voltage measurements are also used to determine the instantaneous maximum and minimum phase voltages (V_{upper} and V_{lower}, respectively). These are then used, along with the modulation index, to determine the duty cycle of the fast switches. The duty cycles, α_+ and α_-, for T_+ and T_-, respectively, are given by:

$$\alpha_+ = M \frac{V_{\text{upper}}}{V_{\text{amp}}} \tag{2}$$

$$\alpha_- = -M \frac{V_{\text{lower}}}{V_{\text{amp}}} \tag{3}$$

3 Simulation

Run the simulation with the model as provided to view the grid-side and load waveforms. The initial output voltage reference is set to $350\,\mathrm{VDC}$. The output and filter capacitors are charged during the first $10\,\mathrm{ms}$ after which the system reaches steady state. The inrush current at startup and that due to step changes in the output voltage and load, excite the resonant frequency of the input filter. This results in the oscillations seen in the current waveforms.

At $t = 0.1\,\mathrm{s}$, the output reference voltage is stepped to $450\,\mathrm{VDC}$. The output capacitor is charged up over the next $4\,\mathrm{ms}$ after which the system reaches its new steady state.

At $t = 0.25\,\mathrm{s}$, the output reference voltage is maintained at $450\,\mathrm{VDC}$ and the load is halved. The output capacitor is discharged over the next $2\,\mathrm{ms}$ and the system again reaches steady state. In the "Load" and "Grid Side" scopes, save the trace and label them "phase-shifted carriers".

Next, change the phase delay of the carrier signal in the controller labeled "CR2" to $0\,\mathrm{s}$. Rerun the simulation and observe the effect of this switching strategy on the output current ripple. This represents the "minimal injection current ripple" switching strategy, while the phase-shifted carriers represent the "minimized dc inductor current ripple" switching strategy proposed by Soeiro. The interval specified in the preconfigured **Saved View** labeled "InjectionCurrent", shows the grid-side currents for the three phases when the injection network switch (SW2) is kept on to inject current into the b-phase (red trace). The effect of the "minimal injection current ripple" switching strategy can be observed when comparing the b-phase grid current for the two proposed switching strategies over the interval specified in the preconfigured **Saved View** labeled "InjectionCurrent_zoomed".

References

[1] Soeiro, T.B.; Friedli, T.; Kolar, J.W., "Swiss rectifier - A novel three-phase buck-type PFC topology for Electric Vehicle battery charging," Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE, pp. 2617-2624, 5-9 Feb. 2012.

[2] Nussbaumer, T.; Heldwein, M.L.; Kolar, J.W., "Differential Mode Input Filter Design for a Three-Phase Buck-Type PWM Rectifier Based on Modeling of the EMC Test Receiver," Industrial Electronics, IEEE Transactions, vol. 53, no. 5, pp. 1649-1661, Oct. 2006.

Revision History:

PLECS 4.3.1	First release
PLECS 4.4.2	Update PI controller component

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PLECS Demo Model