PLECS

DEMO MODEL

Three-Level Boost PFC Converter

Last updated in PLECS 4.4.1

1 Overview

This demonstration presents a single-phase three-level boost power factor correction (PFC) converter. Fig. 1 shows the electrical circuit schematic of the converter. The controller modeled incorporates the PID (proportional-integral-derivative controller) block from the PLECS component library.

System parameters:

- input voltage is $60\,\text{Hz}$, $120\,\text{V}$ AC (rms)
- output voltage is $350\,\text{V}$ DC
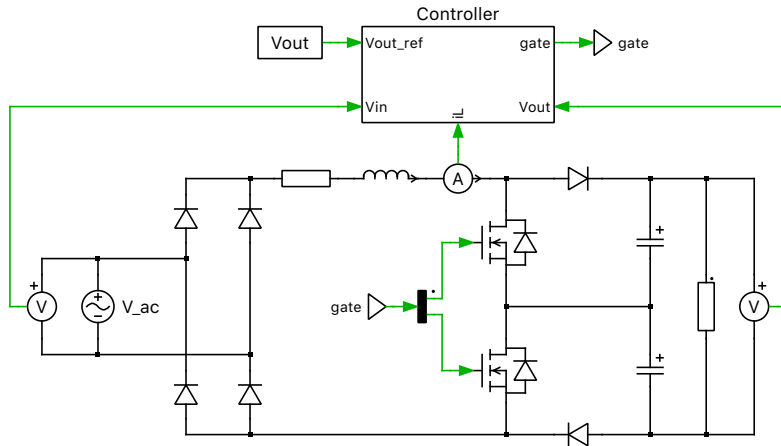- switching frequency is $100\,\text{kHz}$

Figure 1: Electrical circuit of a three-level boost converter

---

Note This model contains model initialization commands that are accessible from:
PLECS Standalone: The menu **Simulation + Simulation Parameters... + Initializations**
PLECS Blockset: Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

---

2 Model

The explanation of the power circuit operation of the three-level boost PFC converter is provided in [1]. With this topology, as compared to the traditional boost PFC circuit, the inductance of the boost inductor can be reduced and the semiconductor device voltage rating is reduced by $50\,\%$ to half of the output voltage. As a result, the converter power density and efficiency can be significantly improved, and design costs can be reduced for high power and/or high voltage applications.

The demo model shows an example power stage that converts single-phase $60\,\text{Hz}$, $120\,\text{V}$ AC (rms) to $350\,\text{V}$ DC.

2.1 Controller

The high-level schematic of the controller implementation is shown in Fig. 2. The voltage compensator regulates the DC bus voltage by comparing the sensed DC output signal against a reference. To prevent the 2nd harmonic DC bus ripple from distorting the input current, a notch filter is added at the input of the voltage compensator. The output of the voltage loop is then multiplied by the rectified input voltage

waveform to generate the current reference. The resulting product is compared against the sensed inductor current. This generated error signal is then used as the input to the current compensator, whose output, the modulation index, m, is then fed to the PWM modulators. The gating signals generated for each of the two switches are offset by $180°$ from the other and the switching frequency is $100\,\mathrm{kHz}$.
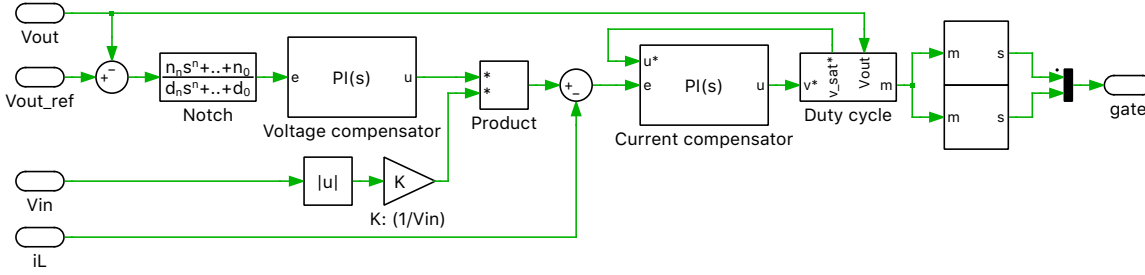

Figure 2: Top-level schematic of control system

Both the voltage and current compensators use the Continuous PID block from the PLECS component library, with the internal design shown in Fig. 3. For more details on this block, consult its documentation from the **Help** button. For the current compensator, the saturation is placed externally to the PID controller block. Also, an internal anti-windup scheme using the Back-Calculation method is enabled.
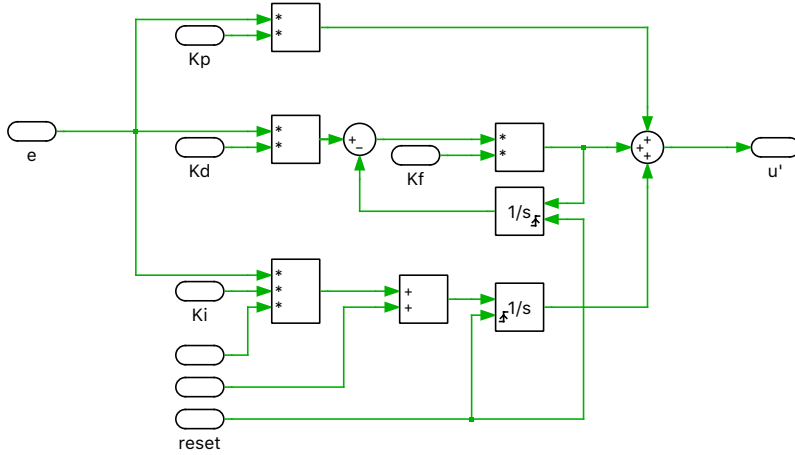

Figure 3: Continuous PID library component implementation

Plant transfer function

To set the PI controller gain parameters a plant transfer function is needed. There are two transfer functions, one for the inner current loop, $C(s)$, and the second one for the outer voltage loop, $V(s)$. The voltage loop is designed to be slower than the current loop so that it does not distort the current reference.

$C(s)$ relates the change of the voltage across the inductor (L) and resistor (R), V_{RL} (the input variable), to the response of the inductor current I_{L} (the output variable):

$$C(s) = \frac{I_{\mathrm{L}}}{V_{\mathrm{RL}}} = \frac{1/R}{1 + s\,L/R} = \frac{K_1}{1 + s\,T_1}, \quad \text{where } K_1 := 1/R \text{ and } T_1 := L/R$$

$V(s)$ relates the change of the current through the inductor (L), I_{L} (the input variable), to the response of the capacitor voltage V_{C} (the output variable):

$$V(s) = \frac{V_{\mathrm{C}}}{I_{\mathrm{L}}} \approx \frac{1}{s\,C} = \frac{1}{s\,T_2}, \quad \text{where } T_2 := C$$

Equivalent delay

The control system often introduces several small delays (e.g. from sensors, actuators, sampling, calculation delays, PWM delay). It is generally assumed that these delays are smaller than the time constant of the plant. If T_Σ is the equivalent delay of the control system, then the simplified transfer function of the delay is:

$$D_\Sigma(s) = \frac{1}{1 + sT_\Sigma}$$

The delays present in this model for this specific implementation are:

- a small time constant for control calculation, T_{calc}, is $\frac{1}{2}\,T_{\mathrm{s}}$
- a small time constant for PWM output generation, T_{pwm}, is $\frac{1}{2}\,T_{\mathrm{s}}$ where, T_{s} is the sample time of the controller.

The equivalent delay, T_Σ, is therefore:

$$T_\Sigma = T_{\mathrm{calc}} + T_{\mathrm{pwm}} = T_{\mathrm{s}}$$

Calculation of control parameters for the current loop

The control parameters of the current PI controller (K_{p} and K_{i}) are calculated using the Magnitude Optimum Criterion. The system's open-loop transfer function $C_{\mathrm{OL}}(s)$ is given by the product of transfer functions from the controller, equivalent time delay and plant:

$$C_{\mathrm{OL}}(s) = \frac{1 + sT_{\mathrm{n}}}{sT_{\mathrm{i}}} \cdot \frac{1}{1 + sT_\Sigma} \cdot \frac{K_1}{1 + s\,T_1}, \quad \text{where } K_{\mathrm{p}} = \frac{T_{\mathrm{n}}}{T_{\mathrm{i}}} \text{ and } K_{\mathrm{i}} = \frac{1}{T_{\mathrm{i}}}$$

The controller parameter T_{n} is chosen such that the pole of the plant transfer function is canceled, i.e. $T_{\mathrm{n}} = T_1$. After this pole-zero cancellation, the closed-loop transfer function represents a second order system. The remaining parameter T_{i} is calculated from setting the damping factor (ζ) of the second order system to $1/\sqrt{2}$, resulting in $T_{\mathrm{i}} = 2K_1T_\Sigma$.

Calculation of control parameters for the voltage loop

The control parameters of the voltage PI controller (K_{p} and K_{i}), since the outer voltage loop of the plant represents a pure integrator, are calculated using the Symmetrical Optimum Criterion. The system's open-loop transfer function $V_{\mathrm{OL}}(s)$ is given by the product of the transfer functions of the controller, equivalent time delay and plant:

$$V_{\mathrm{OL}}(s) = \frac{1 + sT_{\mathrm{n}}}{sT_{\mathrm{i}}} \cdot \frac{1}{1 + sT_\Sigma} \cdot \frac{1}{s\,T_2}, \quad \text{where } K_{\mathrm{p}} = \frac{T_{\mathrm{n}}}{T_{\mathrm{i}}} \text{ and } K_{\mathrm{i}} = \frac{1}{T_{\mathrm{i}}}$$

After solving the corresponding closed-loop transfer function, the final coefficients are:

$$T_{\mathrm{n}} = 4 \cdot T_\Sigma \text{ and } T_{\mathrm{i}} = 8 \cdot \frac{T_\Sigma{}^2}{T_2}$$

For a more detailed explanation on calculating the controller parameters, refer to [2].

3   Simulation

Run the simulation with the model as provided to observe the PWM signals, as well as the input AC current, load DC voltage and inductor current, as shown in Fig. 4 and Fig. 5, respectively. At steady state, the ripple in the output voltage and the total harmonic distortion (THD) of the input current can be measured using the Cursors button at the top of the Scope. Alternatively, THD can also be measured using the THD block from the PLECS component library.

Observations:

- PWM signals offset by $180°$, as seen in Fig. 4

- The input current (red) and scaled input voltage (green) waveforms in the second plot of Fig. 5 can be observed as being almost in phase
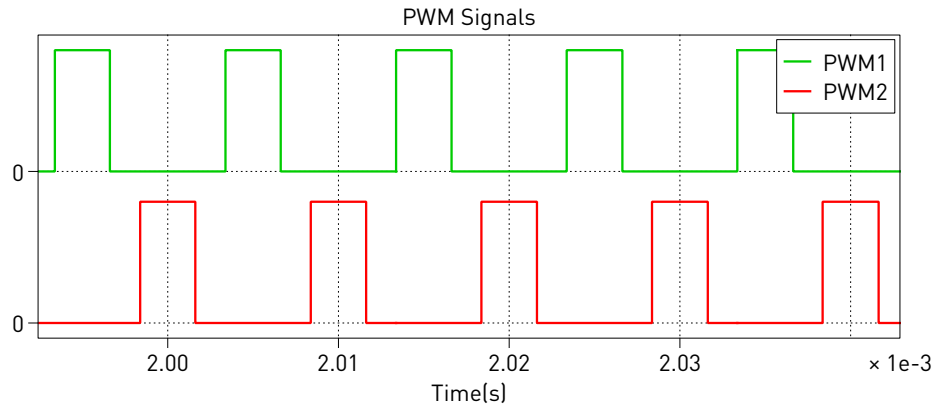- The resulting THD of the input current is $4.75\,\%$.
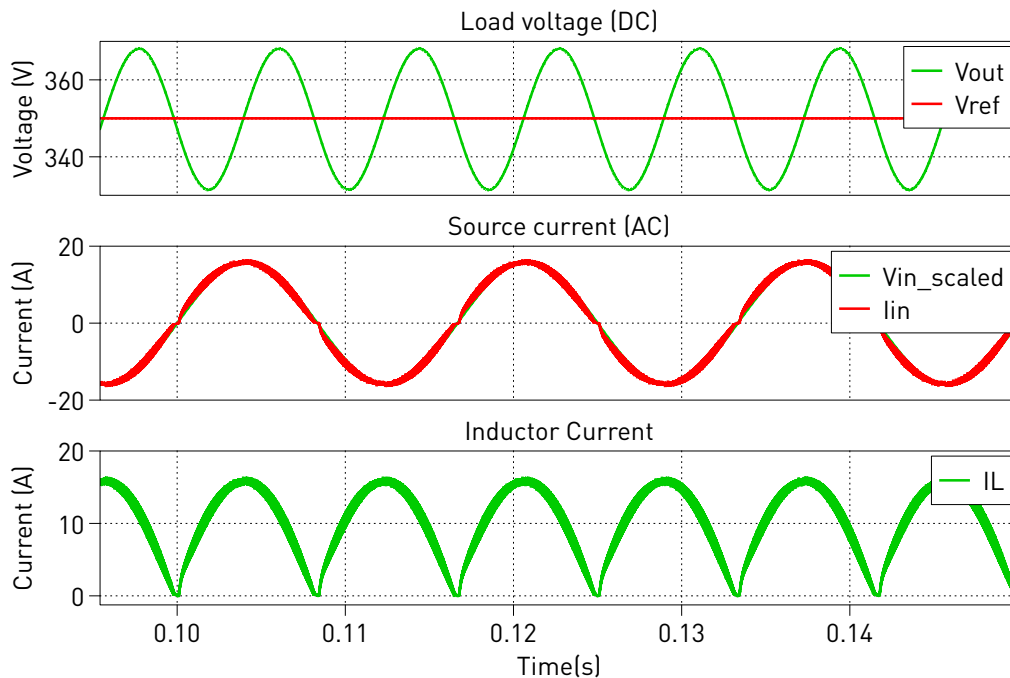

Figure 4: PWM signals

Figure 5: Load voltage (DC), input current (AC) and inductor current

4   Conclusion

This model highlights a three-level boost PFC converter. It makes use of the PID Controller block from the PLECS component library.

References

[1] M. T. Zhang, Yimin Jiang, F. C. Lee and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," Proceedings of *1995 IEEE Applied Power Electronics Conference and Ex-*

position - APEC'95, Dallas, TX, USA, 1995, pp. 434-439 vol.1. Click to access online: IEEE Xplore webpage.

[2] Conception de Systèmes automatiques, Hansruedi Bühler, Presses Polytechniques Romandes, Lausanne 1988, ISBN 2-88074-149-1

Revision History:

PLECS 4.4.0   First release

How to Contact Plexim:

☎	+41 44 533 51 00	Phone
	+41 44 533 51 01	Fax
✉	Plexim GmbH Technoparkstrasse 1 8005 Zurich Switzerland	Mail
@	info@plexim.com	Email
	http://www.plexim.com	Web

PLECS Demo Model