

PLECS

DEMO MODEL

Three-Phase T-Type Inverter

Last updated in PLECS 4.6.1

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1 Overview

This demonstration presents a three-phase T-type inverter for grid-tie applications that deploys Wolf-speed SiC MOSFETs. Fig. 1 shows the electrical circuit of the T-type inverter. This model exhibits how the device selection, controller parameters, and modulation approach influence the thermal performance of the inverter. By leveraging analysis tools and simulation scripts, the inverter performance is studied under several different operating conditions to ensure the system operates safely and efficiently.

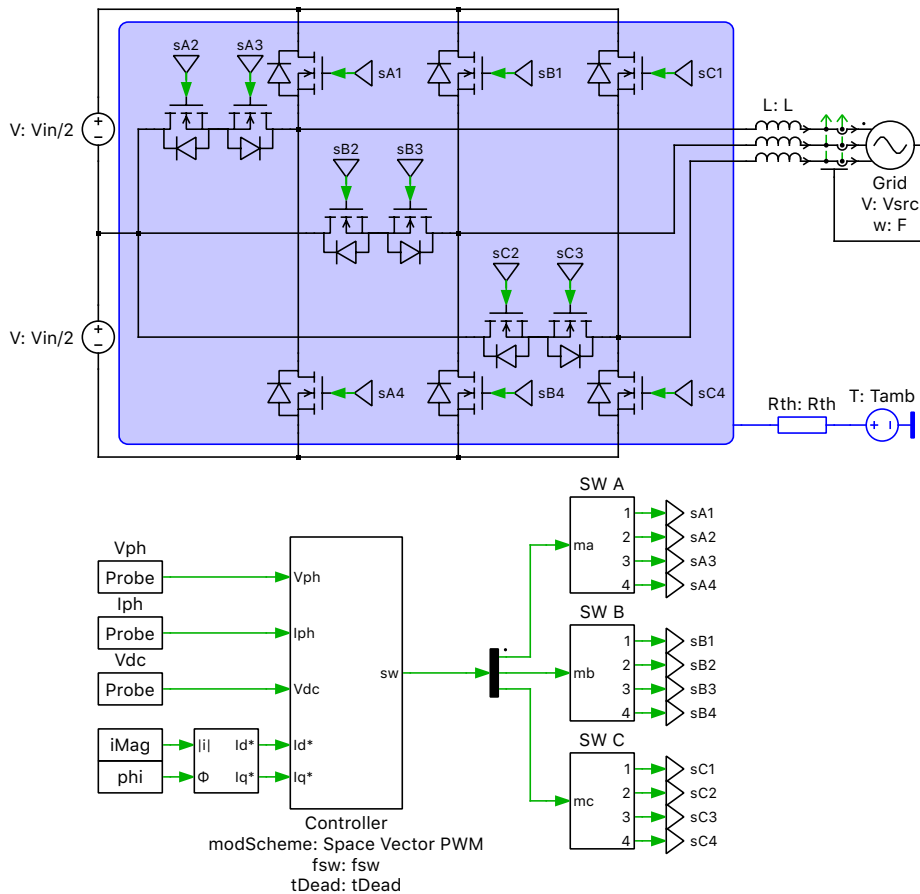


Figure 1: Electrical circuit of a three-phase T-type inverter

2 Model

The T-type inverter is similar to the three-level neutral-point clamped (NPC) inverter in that it adds an additional output voltage level at 0V, thereby offering improved harmonic performance over a standard two-level inverter. Compared to an NPC inverter, the T-type inverter has a reduced part count due to the elimination of the clamping diodes, and reduced conduction losses of the outer switching devices, since only one device is used rather than two in series [1]. The disadvantage is that the blocking voltage is reduced compared to the NPC inverter since the outer switching devices are no longer in series. This can be overcome with modern wide-bandgap devices.

The demo model shows an example of a T-type inverter rated at 22 kVA that converts an 800 V DC-bus into a three-phase 60 Hz, 480 V (line-line, rms) distribution for industrial applications.

2.1 Thermal

All 12 devices are configured to demonstrate the thermal loss performance of different Wolfspeed SiC MOSFETs. For the T-type inverter, it is common to have different switch types or even switch technology for the outer switches and neutral point-connected switch pair [1, 2]. The device types and parameters are defined in the **Model initialization commands** in the **Initializations** tab of the **Simulation + Simulation Parameters...** window. The outer switches and neutral-connected switches are defined separately to evaluate how the switch selection impacts the thermal performance of the inverter.

The model is configured with the device data for three different switch types, with the values below referenced to a junction temperature of 25 °C:

- C3M0065100K SiC MOSFET rated for 1000 V/35 A operation with an R_{dsOn} of 65 m Ω
- C3M0032120K SiC MOSFET rated for 1200 V/65 A operation with an R_{dsOn} of 32 m Ω
- C3M0021120K SiC MOSFET rated for 1200 V/100 A operation with an R_{dsOn} of 21 m Ω

Alternatively, you can specify another Wolfspeed (or other vendor's) device.

Each semiconductor device is modeled as a subsystem with a custom mask configuration. The subsystem consists of a separate MOSFET and body diode, each with their own thermal model. The component mask has settings for several datasheet parameters such as on-resistances and body diode forward voltages. Specifying these parameters is important as it determines if the current is flowing through the MOSFET, body diode, or both conduction paths. This in turn can influence the switch losses. You also have the option to configure the gate resistance R_g (consult with the manufacturer for recommended values), which will effect the switching loss calculation, as well as the number of devices specified in parallel. By increasing the number of parallel devices, it is possible to scale up the power requirements of the system and reduce the per-device stresses.

For more information on thermal modeling and the calculation of device losses and efficiency, see the demo model “Buck Converter with Thermal Model” in the PLECS demo models library.

Device Assertions

The maximum operating conditions of drain-source voltage V_{ds} , drain current I_{ds} , and junction temperature T_j for each device are entered from the manufacturer's datasheet. The measured values during the simulation are compared with the rated values and are used to generate assertions, as shown in Fig. 2. A one-dimensional look-up table is used to dynamically adjust the continuous drain current limit as a function of case temperature $I_{ds}(T_c)$. Fig. 3 shows a comparison between the look-up tables for the different devices, as extracted from the device datasheet. The assertions will generate warnings to alert the user if the device is operating outside of the safe operating area, as configured in the **Assertion action** setting in the **Options** tab of the **Simulation + Simulation Parameters...** window.

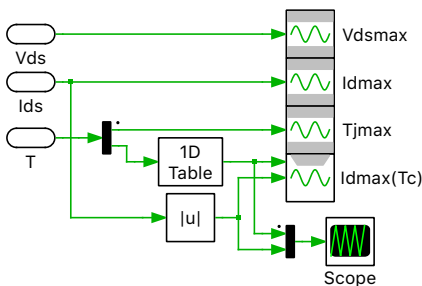


Figure 2: Implementation of thermal assertions

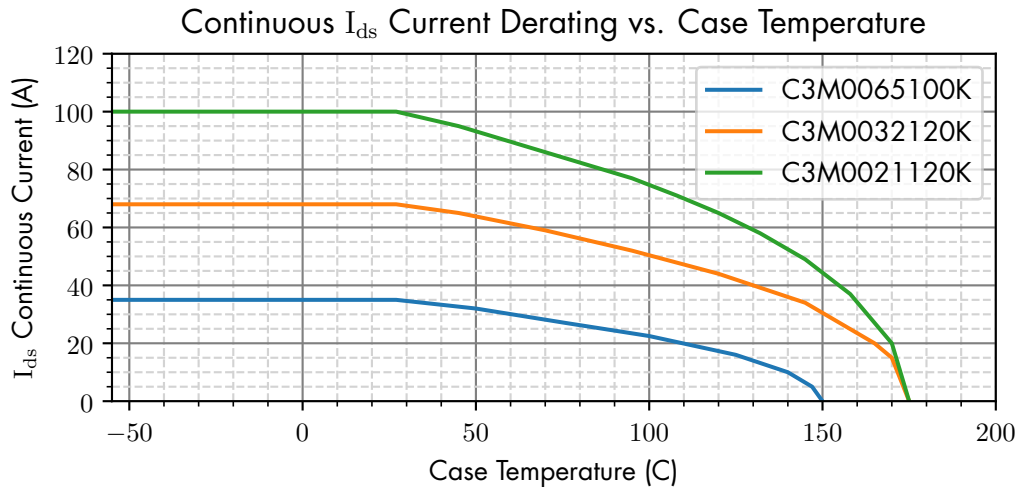


Figure 3: Continuous drain current limit vs. case temperature for several devices

2.2 Controller

The high-level schematic of the controller implementation is shown in Fig. 4.

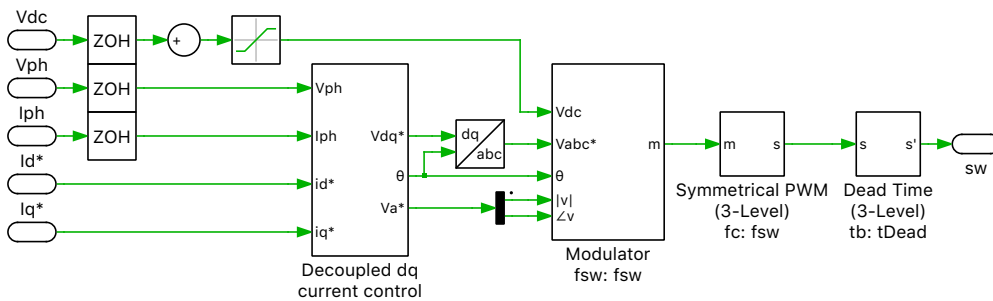


Figure 4: Top-level schematic of control system

A decoupled synchronous reference frame current controller, shown in Fig. 5, is used to generate a dq voltage reference V_{dq}^* for the modulator. The dq current controller regulates the inverter output currents to the desired set points, with separate PI regulators for direct and quadrature currents. The PI controllers include decoupling feedforward terms for the main output inductance. The phase angle for the voltage reference is measured using a simple synchronous reference frame phase-locked loop (PLL). The V_{dq}^* voltage reference value is converted to a three-phase voltage reference V_{abc}^* using the PLL's angle output. V_{abc}^* is fed into a the modulator, where the user can selection between different modulation schemes. The resulting modulation index, m , is then used to generate a switching function with an optional dead time. Lastly, the switch signals are generated for each of the three inverter legs, as was shown in Fig. 1.

The “Modulator” component is implemented as a Configurable Subsystem. Since the modulation approach can significantly impact the semiconductor losses, different modulation approaches are implemented so they can be benchmarked against each other [2]. The simplest modulation scheme is classical Sinusoidal Pulse Width Modulation (SPWM). The key drawback of the SPWM approach is that the inverter does not fully utilize the available DC-bus voltage; the modulation is linear only between ± 1.0 times the DC-bus voltage. Zero sequence injection approaches are used such that the linear range of the modulation index is extended to $\pm 2/\sqrt{3}$ the DC-bus voltage [4].

A generic modulation signal $e_i(t)$ can be divided into a component associated with the fundamental sinusoid $e_i^*(t) = m_i \cdot \sin(\omega t + \phi_i)$ and a component associated with the zero sequence injection $e_i^0(t)$, where the i subscript indexes each electrical phase of the converter and ϕ_i is the associated phase shift. Since

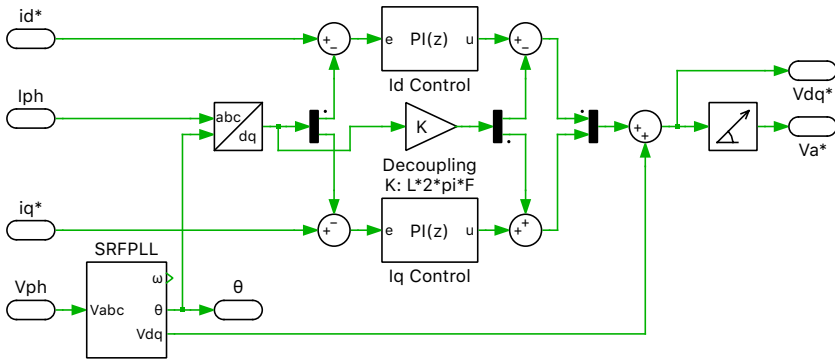


Figure 5: Synchronous reference frame current controller implementation

the injected signal is zero sequence, it means that a common signal is injected into all three phases and $e_a^0(t) = e_b^0(t) = e_c^0(t)$. This model compares basic SPWM, where $e_i^0(t) = 0$, with simple Space Vector PWM (SVPWM), Third Harmonic Injection PWM (THIPWM), Third Harmonic Zero Sequence PWM (THZSPWM), and Discontinuous PWM (DPWM) [2, 4]. The simplified SVPWM and DPWM are based on comparing the minimum and maximum thresholds of the modulation indices to each phase. The THIPWM and THZSPWM approaches use the converter's PLL to define the phase for the injected signal, where the THZSPWM is a sinusoidal approximation of the SVPWM waveform. Fig. 6 shows a comparison of different zero sequence injection waveforms along with a SPWM reference signal.

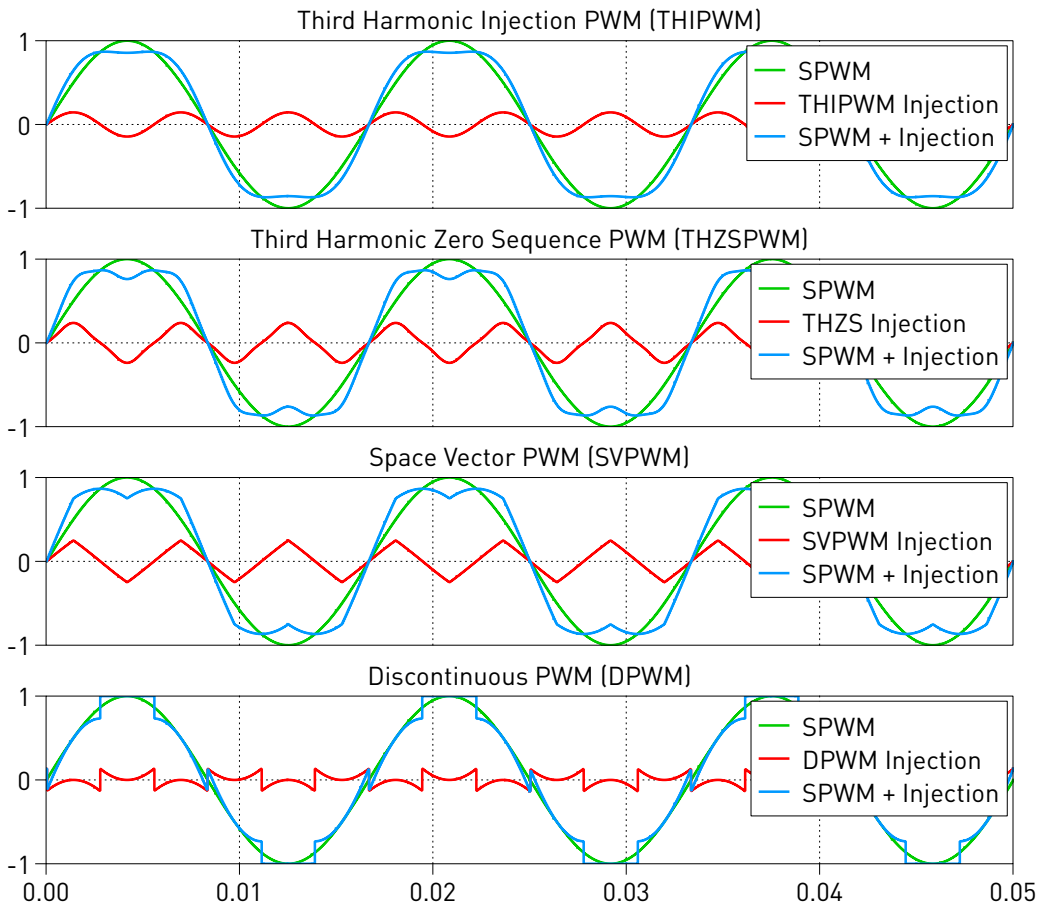


Figure 6: Comparison of different zero sequence injection methods

3 Simulation

Run the simulation with the model as provided to observe the PWM signals for each phase leg, the output AC currents, the signals for devices S_{11} and S_{12} , and the calculated losses of the system. Since the system will reach its final thermal operating point much slower than its electrical one, running the preconfigured **Steady-State Analysis**, accessible from the **Simulation + Analysis tools...** menu is recommended. The script is by default configured to compare SPWM and SVPWM modulation schemes, but different modulation indices can be compared by setting the `modAnalyzeIdxs` variable in the script.

In addition to the system-level electrical specifications, you can experiment with the controller settings by manipulating the modulation scheme, switching frequency, dead time, controller set points, and controller gains. Similarly, the device type, number of parallel devices, and the impact of external cooling or larger heatsinks could be analyzed. All of these settings will impact the loss behavior and system efficiency. If a device is operating outside of the safe operating area, a warning icon ⚠ will appear in the bottom right hand of the simulation window, identifying which operating criteria was violated. The losses and the maximum continuous drain current I_{ds} are both temperature-dependent and therefore are best assessed when all the thermal dynamics have reached a steady-state operating point.

3.1 Parameter sweep and simulation script

Since the power converter losses are sensitive to a large number of variables, a parameter sweep is an effective way to determine how design decisions impact the converter performance over a range of operating conditions. A simulation script is configured in the **Simulation + Simulation scripts...** that compares the different modulation approaches at peak current output for varying power factor angles. The script runs a Steady-State Analysis for each case, since the losses are sensitive to the steady-state device temperatures.

The simulation script in PLECS Blockset simulates each operating condition sequentially. In PLECS Standalone, the simulation script runs several simulations in parallel. Refer to the “Buck Converter with Parameter Sweep” in the PLECS demo models library for a more comprehensive explanation of the parallel simulation scripting feature.

The results of the parameter sweep are shown in Fig. 7 where a single C3M0021120K is chosen for the outer switches and two parallel C3M0065100K devices are chosen for the neutral-connected switches. The topmost plot shows the overall losses of the power converter, while the bottommost plot shows the device junction temperatures for one outer switch and one neutral-connected switch. Each run that has an assertion is marked with a red cross (x), indicating the device operated outside of the safe operating area during the simulation. As of PLECS 4.4, Octave plots can be generated within a PLECS Standalone simulation script or initialization script. Fig. 7 was generated directly in PLECS from the results of the parameter sweep. Alternatively, the results can be exported in other formats supported by Octave, such as `*.mat` or `*.csv`.

One can observe that at unity power factor DPWM has the lowest losses, followed by SPWM. However, when the power factor angle approaches normalized power factor angles of 0.5, these two methods show the highest losses, and the neutral-connected devices will operate outside of the safe operating area. The SVPWM approach shows a 15 % reduction in losses compared to DPWM for the same operating scenario. One proposed technique is to dynamically adjust the modulation strategy based on the operating conditions to achieve the lowest overall losses [2].

4 Conclusion

This model highlights a three-phase T-type inverter for an industrial distribution network application. It makes use of simple plant and controller designs in order to highlight the thermal modeling capabilities of PLECS. This model can serve as an example for studying controller design influence on efficiency for other topologies.

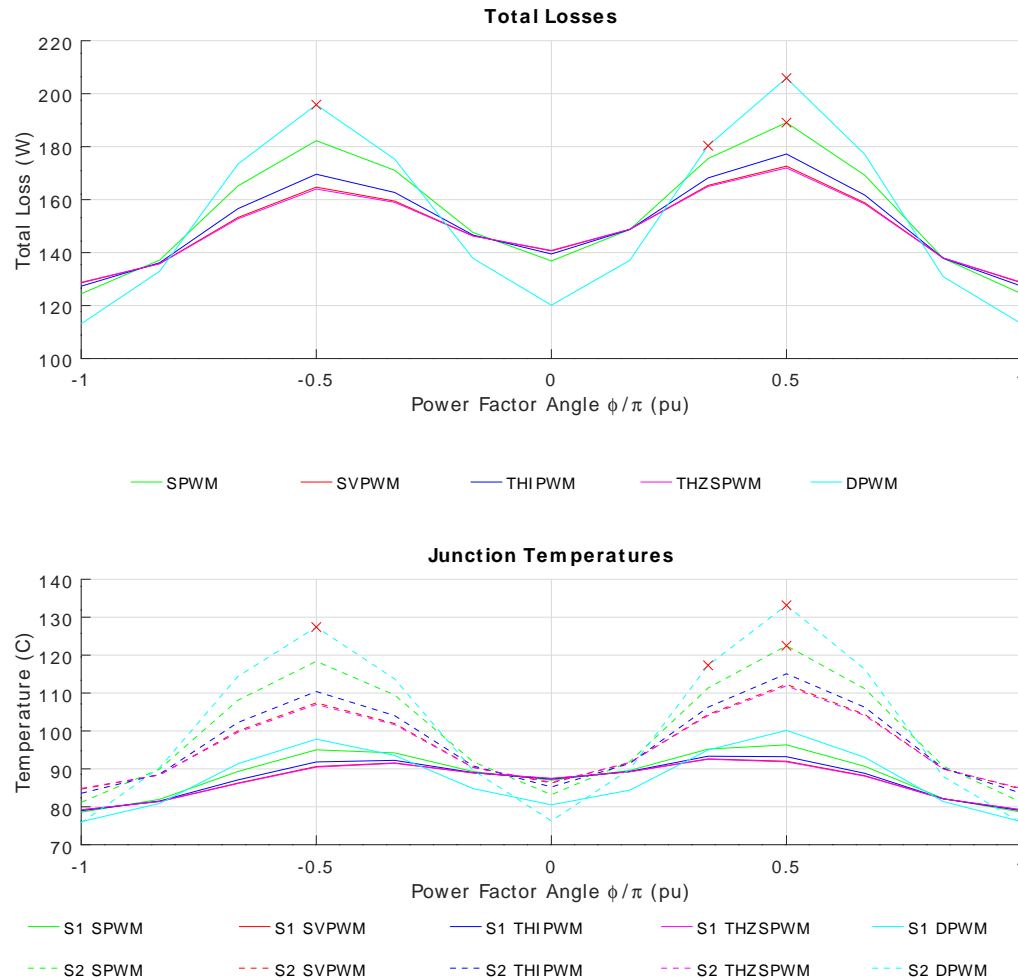


Figure 7: Total losses and device temperatures for different modulation schemes

References

- [1] M. Schweizer and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," in *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 899-907, Feb. 2013. Click to access online: [IEEE Xplore webpage](#).
- [2] E. Serban, C. Pondiche, and M. Ordonez, "Power-loss analysis in 3-level TNPC inverters: Modulation effects," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 490-497. Click to access online: [IEEE Xplore webpage](#).
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- [4] K. Zhou and D. Wang, "Relationship between space-vector modulation and three-phase carrier-based PWM: a comprehensive analysis three-phase inverters," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 1, pp. 186-196, Feb. 2002. Click to access online: [IEEE Xplore webpage](#).

Revision History:

PLECS 4.4.1	First release
PLECS 4.6.1	Update PLECS Standalone simulation script to utilize the parallel simulation feature.

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