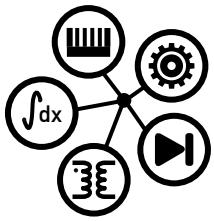

# RT Box

## *DEMO MODEL*

**Minimal Example Demos**

Last updated in RT Box Target Support Package 3.0.3

**www.plexim.com**

- Request a PLECS and PLECS Coder trial license
- Get the latest RT Box Target Support Package
- Check the PLECS and RT Box documentation

# 1 Overview

These RT Box minimal example demos feature basic power converter topologies running on a single RT Box. These demo models have the following features:

- The converter topologies are built with components under PLECS library Power Modules, in their default `Sub-cycle average` or `Sub-step events` configuration.
- The PWM signal generation uses a simple open-loop pattern, on the same RT Box where the converter topology runs in real-time.
- To deploy the model on a single RT Box, a loopback cable is needed to connect together the Digital Out interface and the Digital In interface at the front panel of the Box.

This document describes a common concept of the minimal example demos. It focuses on showcasing the execution capability of the RT Box for basic converter topologies. Please note that here is no intention of providing actual parameters for a real-world converter design.

The chosen discretization step size and average execution time for CPU, and the FPGA step size of each minimal example demo are shown in Tab. **??**.

**Table 1: Discretization step size and average execution time of the minimal example demos**

| Model<br>Name | RT Box 1<br>CPU exec. time / step size | RT Box 2 or 3<br>CPU exec. time / step size, FPGA step |
|---|---|---|
| Buck Converter | 0.85 $\mu$s / 1.25 $\mu$s | 1.5 $\mu$s / 2 $\mu$s , 400 ns |
| Boost Converter | 0.9 $\mu$s / 1.25 $\mu$s | 1.5 $\mu$s / 2 $\mu$s , 400 ns |
| Single-Phase Inverter | 1.2 $\mu$s / 1.5 $\mu$s | 1.8 $\mu$s / 2 $\mu$s , 400 ns |
| Three-Phase Inverter | 1.8 $\mu$s / 2 $\mu$s | 1.9 $\mu$s / 2.5 $\mu$s , 417 ns |
| Three-Level NPC Inverter | 2.2 $\mu$s / 2.5 $\mu$s | 2 $\mu$s / 2.5 $\mu$s , 417 ns |
| Three-Level NPC Inverter<br>(two interleaved branches with breakers) | 5 $\mu$s / 5.5 $\mu$s | 2.2 $\mu$s / 2.5 $\mu$s , 500 ns |
| Three-Level T-Type Inverter | 2.3 $\mu$s / 2.5 $\mu$s | 1.9 $\mu$s / 2.5 $\mu$s , 417 ns |
| Three-Level ANPC Inverter | 2.5 $\mu$s / 3 $\mu$s | 2.1 $\mu$s / 2.5 $\mu$s , 417 ns |
| Five-Phase Inverter | 3 $\mu$s / 5 $\mu$s | 2 $\mu$s / 5 $\mu$s , 385 ns |
| Five-Phase Interleaved Sync. Buck | 2 $\mu$s / 3.5 $\mu$s | 1.6 $\mu$s / 2.5 $\mu$s , 417 ns |
| Flying-Cap Single-Phase Inverter | 4.4 $\mu$s / 6 $\mu$s | 2.5 $\mu$s / 4.5 $\mu$s , 450 ns |
| Cascaded Full-Bridge Rectifier | 5.9 $\mu$s / 6 $\mu$s | 2.6 $\mu$s / 4.5 $\mu$s , 900 ns |
| Dual-Active Bridge | 1.6 $\mu$s / 2 $\mu$s | 1.6 $\mu$s / 2 $\mu$s , N/A |
| Half-Bridge LLC | 1.3 $\mu$s / 1.88 $\mu$s | 1.5 $\mu$s / 1.88 $\mu$s , N/A |
| Full-Bridge LLC | 1.6 $\mu$s / 1.88 $\mu$s | 1.6 $\mu$s / 1.88 $\mu$s , N/A |
| Phase-Shifted Full-Bridge | 1.55 $\mu$s / 1.8 $\mu$s | 1.6 $\mu$s / 1.8 $\mu$s , N/A |

## 1.1 Requirements

To run these demos, the following items are needed (available at `www.plexim.com`):

- PLECS and PLECS Coder license, min. version 4.8.1 required

- One PLECS RT Box CE, 1, 2 or 3
- The RT Box Target Support Package, min. version 3.0.1 required
- Follow the step-by-step instructions on configuring PLECS and the RT Box in the Quick Start guide of the RT Box User Manual
- One 37 pin Sub-D cable

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**Note** This model contains model initialization commands that are accessible from:

*PLECS Standalone:* The menu **Simulation + Simulation Parameters... + Initializations**

*PLECS Blockset:* Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

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# 2 Model

Since all the minimal example demos follow the same self-loopback concept, below we use the Flying-Capacitor Single-Phase Inverter model for illustration. Fig. **??** depicts the top-level schematic of the minimal example model.

The users can add a Scope at the top-level schematic to visualize the generated ideal PWM signals in an offline simulation on the PC.

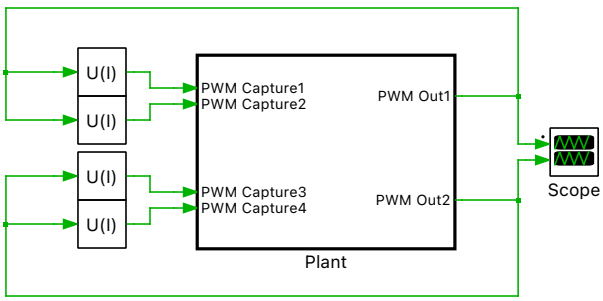


**Figure 1: Top-level schematic of a minimal example demo**

The “Plant” Subsystem includes both the converter topology and the PWM generation logic. Fig. **??** shows the circuit model inside the “Plant” Subsystem.

## 2.1 Converter topology

The converter’s switching legs are built with components under PLECS library Power Modules, in their default configuration: `Sub-cycle average` (for non-isolated topologies) or `Sub-step events` (for isolated DC-DC topologies).

The `Assertions` inside the Power Modules are all configured as the default **On**. During real-time running, an overlapping in gating signals of the complementary switch pair can be caught. RT Box will throw an error message.

An Electrical Model Settings block is connected to the converter bridge leg. Inside this block, the **Target** can be chosen as **CPU** or **FPGA**.

- CPU - available on all RT Boxes, also the default option for building onto an RT Box 1.
- FPGA - only available on RT Box 2 and 3, therefore the default option for building onto an RT Box 2 or 3.

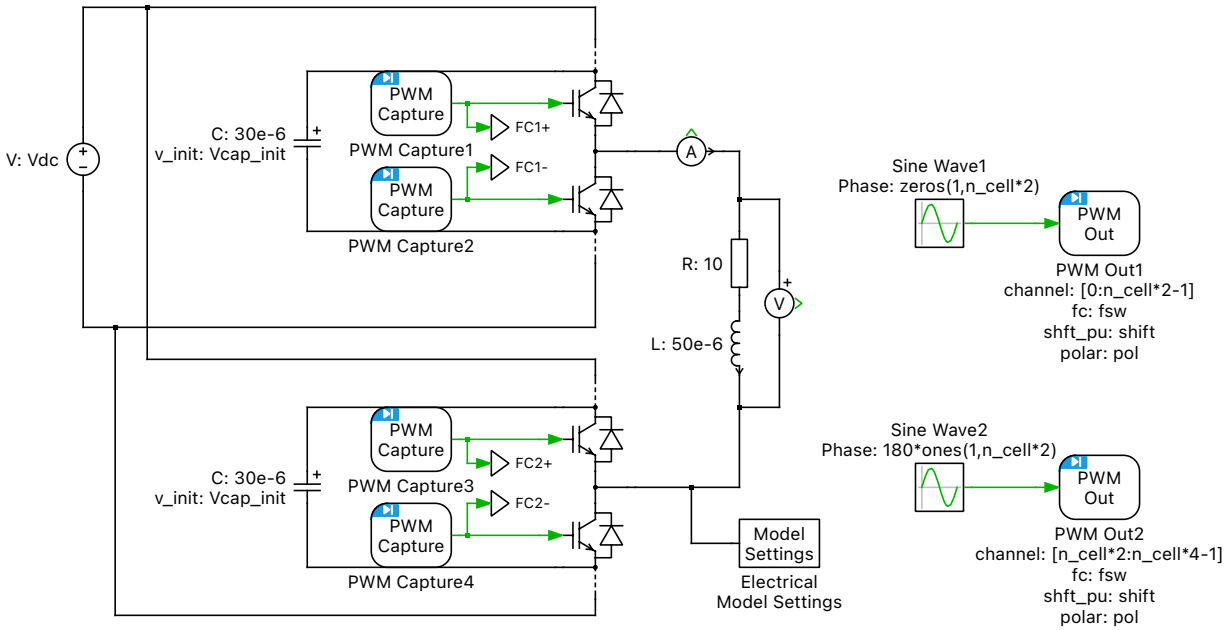


**Figure 2: Plant subsystem schematic of a minimal example demo**

Also, the discretization step size `Ts_plant` may be adjusted slightly between different simulation targets. Please see the model initialization commands of each demo for more details.

## 2.2 PWM generation and capturing

PWM Out blocks from the RT Box target support library are used to generate PWM signals. Configurations such as `Carrier phase shift`, `Carrier limits`, or `Polarity`, are utilized to generate gating signal patterns for different topologies in a versatile way on the RT Box.

PWM Capture blocks from the RT Box target support library are used to sample in the self-generated PWM signals in the loopback way. Note that for FPGA simulation, a prerequisite is that the PWM Capture blocks have to be connected directly to the gates of the Power Modules - this is already the case in all minimal exmaple demo implementation.

# 3 Simulation

Please follow the instructions below to deploy a minimal example model onto a single RT Box:

1. Connect the Digital Out interface to the Digital In interface of a single RT Box, using a DB37 cable shown in Fig. **??**.
2. From the **System** tab of the **Coder options...** window, select the “Plant” and **Build** it onto the user’s RT Box.
3. Once the model is uploaded, from the **External Mode** tab of the **Coder options...** window, **Connect** to the RT Box and **Activate autotriggering**.
4. The user can view the real-time waveforms from the Scopes connected inside the “Plant” subsystem schematic.
5. The user can also find more CPU or FPGA simulation real-time performance information under the **Application** and **Diagnostics** tabs of the RT Box Web Interface.

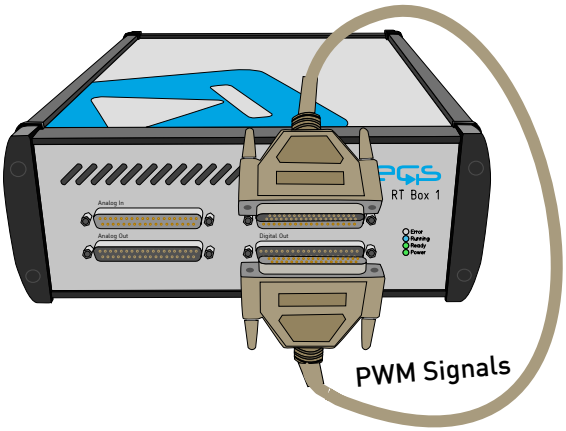


**Figure 3: Single RT Box with a loopback cable connected in front to run the minimal example demos**

# 4 Conclusion

These minimal example demos showcase the simple usage of a single RT Box in PWM signal loopback setup. CPU or FPGA simulation can be configured in the PLECS model with the corresponding setting of the Electrical Model Settings block.

**Revision History:**

| | |
|---|---|
| RT Box TSP 3.0.1 | First Release |
| RT Box TSP 3.0.3 | Add the NPC inverter demo with two interleaved branches |

**How to Contact Plexim:**


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*RT Box Demo Model*