RT Box LaunchPad Interface

User Manual May 2020

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RT Box LaunchPad Interface

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Introduction

The PLECS RT Box 1 is a powerful real-time simulator based on a 1 GHz Xilinx Zynq system on a chip (SOC). With its 64 digital and 32 analog I/O signals, the RT Box is well equipped for hardware-in-the-loop (HIL) testing as well as rapid control prototyping.

If employed for HIL testing the RT Box typically emulates the power stage of a power electronic system. The power stage could be a simple DC/DC converter, an AC drive system or a complex multi-level inverter system. The device under test (DUT) is the control hardware connected to the RT Box. In such a setup, the complete controller can be tested without the real power stage.

To simplify the connection of external hardware and to provide convenient access to the RT Box inputs and outputs, Plexim offers a set of RT Box accessories.

The **RT Box LaunchPad Interface** described in this document facilitates a simple connection of the RT Box with the LaunchPad and LaunchPad XL development kits from Texas Instruments. It enables the user to test control algorithms implemented on C2000 MCUs without developing their own interface hardware. The pinout of the LaunchPad Interface board has been optimized for the following development kits:

- LaunchXL-F28069M
- LaunchXL-F28377S
- LaunchXL-F28379D
- LaunchXL-F28027

The LaunchPad Interface may also be used with other development boards compliant with the LaunchPad pinout.

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Interface Board Overview

The LaunchPad Interface board facilitates the connection between a LaunchPad from TI with a C2000 microcontroller and the RT Box. Fig. 2.1 shows the top view of the board without any LaunchPad attached.

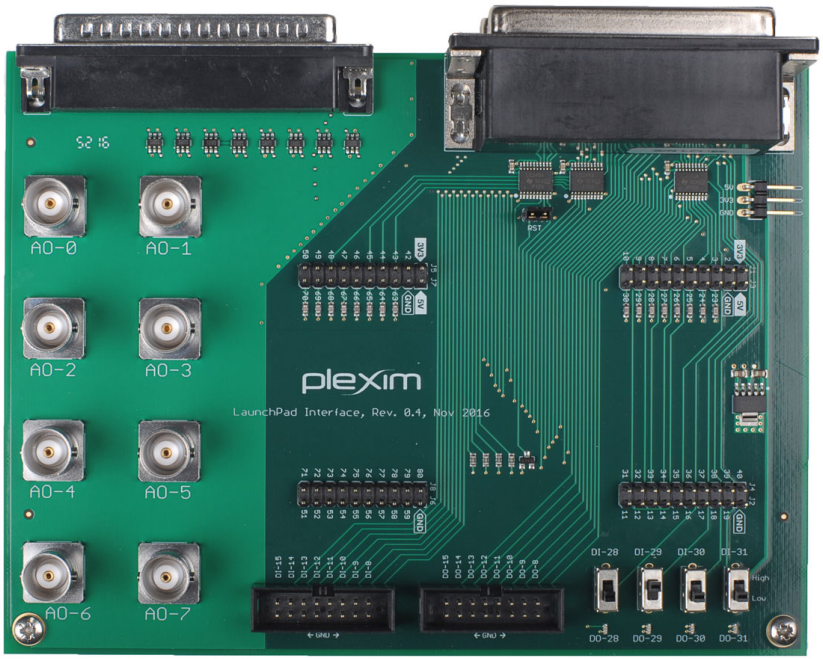

Figure 2.1: Top view of RT Box LaunchPad Interface

Additionally, the board provides access to some of the analog outputs of the RT Box via BNC connectors and to unused digital inputs and outputs signals via shrouded pin headers. For simple status communication with the RT Box the board features four sliding switches and four LEDs.

Fig. 2.2 shows the top view of the board with a LaunchXL-F28069M attached.

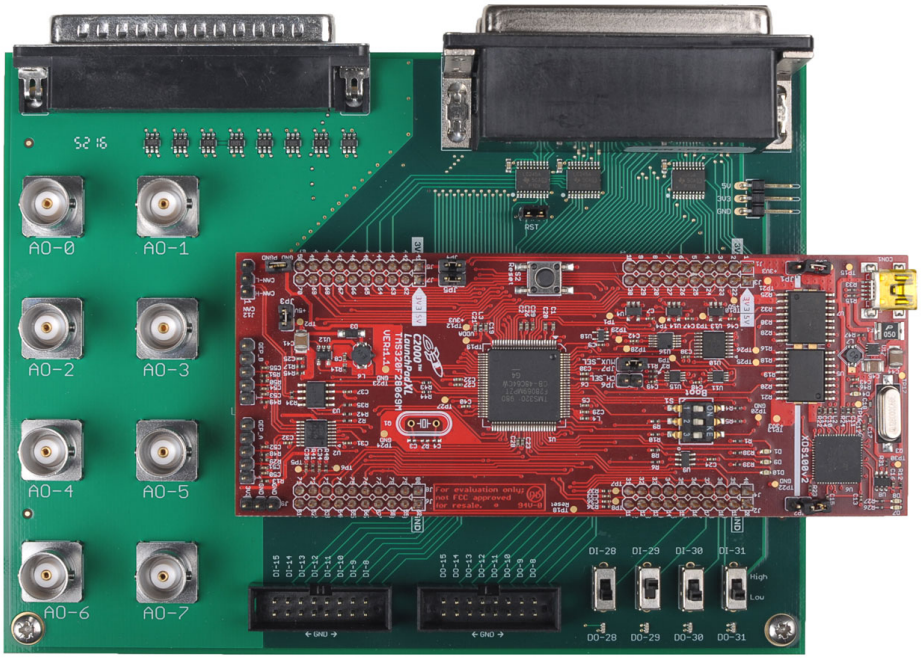

Figure 2.2: RT Box LaunchPad Interface with LaunchXL-F28069M

Fig. 2.3 shows the top view of the board with a LaunchXL-F28027 attached.

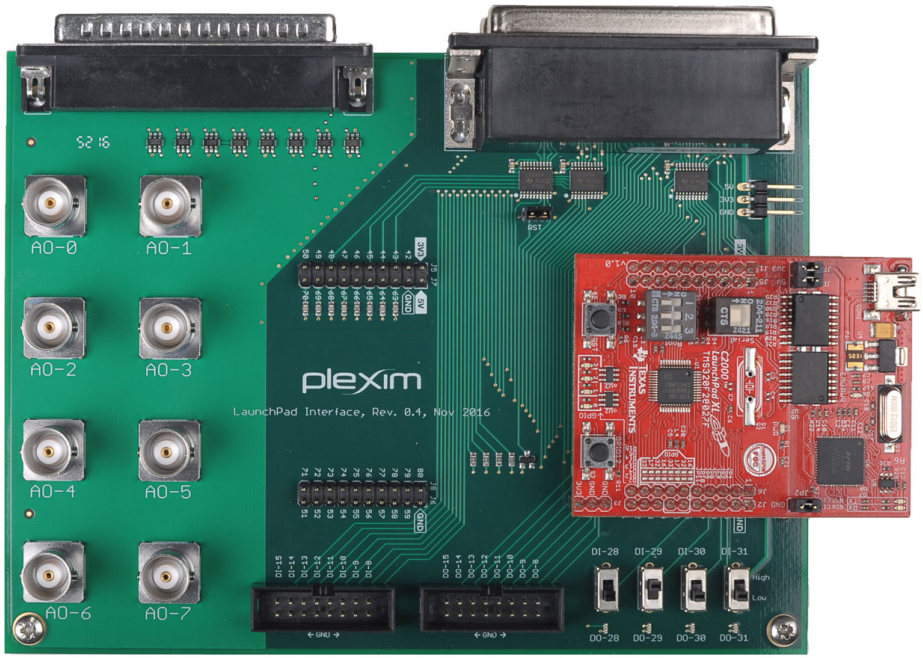

Figure 2.3: RT Box LaunchPad Interface with LaunchXL-F28027

LaunchPad Headers

A LaunchPad must be attached to the Interface board using the corresponding pin headers. The LaunchPad will extend beyond the edge of the Interface board. Fig. 2.2 and 2.3 show the correct mounting position.

Tables 2.1 and 2.2 list the pin assignments of the LaunchPad headers and the RT Box signals.

RT Box	Header		RT Box
	J1	J3	
3.3 V	1	21	
	2	22	GND
DO0	3	23	AO0
DO1	4	24	AO1
DO2	5	25	AO2
	6	26	AO3
DI24	7	27	AO4
DI25	8	28	AO5
DI26	9	29	AO6
DO27	10	30	AO7

RT Box	Header		RT Box
	J4	J2	
DI0	40	20	GND
DI1	39	19	DI6
DI2	38	18	DI7
DI3	37	17	
DI4	36	16	DO25
DI5	35	15	DI27
DO4	34	14	DO26
DO5	33	13	DO6
	32	12	DO7
	31	11	DO3

Table 2.1: LaunchPad header pins J1-J4

A more detailed table including the available processor functions at each pin for the supported LaunchPads can be found in the appendix.

Onboard Voltage Supply

As the LaunchPad is powered from the interface board no external power supply is required. The interface board contains a linear voltage regulator that converts the 5 V supplied by the RT Box down to 3.3 V required by the LaunchPad.

RT Box	Header		RT Box
	J5	**J7**	
3.3 V	**41**	**61**	
	42	**62**	GND
DO16	**43**	**63**	AO8
DO17	**44**	**64**	AO9
DO18	**45**	**65**	AO10
	46	**66**	AO11
	47	**67**	AO12
DO19	**48**	**68**	AO13
	49	**69**	AO14
	50	**70**	AO15

RT Box	Header		RT Box
	J8	**J6**	
DI16	**80**	**60**	GND
DI17	**79**	**59**	DI22
DI18	**78**	**58**	DI23
DI19	**77**	**57**	
DI20	**76**	**56**	
DI21	**75**	**55**	DO20
	74	**54**	DO21
	73	**53**	DO22
	72	**52**	DO23
	71	**51**	DO24

Table 2.2: LaunchPad header pins J5-J8

The pins labeled *5 V* at pin headers *J1* and *J5* of the interface board are supplied with 5 V generated by the TI launchpad. Therefore, a 5 V output at these pins is only available when a TI launchpad is present.

Both supply voltages *5 V* and *3.3 V* are accessible at a 3-pin header on the interface board if the user wants to power external circuits. The maximum load for both voltage levels combined is 1.5 A. When an external circuit requires a 5 V supply it is recommended to draw the required power from the 3-pin header on the interface board and not from the LaunchPad in order to minimize losses and component stress.

Analog Output

The interface board connects all 16 analog outputs from the RT Box to the LaunchPad headers. The lower 8 channels *AO0*...*AO7* are also accessible at the BNC connectors. Each of the analog output channels is clamped with two Schottky diodes to 0 V and 3.3 V to protect the inputs of the MCU from damage by overvoltage.

To stabilize the analog voltages for the sample and hold capacitors inside the MCU, each channel is buffered with a 220 pF capacitor against ground.

Digital I/O

Not all of the digital inputs and outputs of the RT Box are connected to the LaunchPad. The unused digital inputs *DI8*...*DI15* and the outputs *DO8*...*DO15* are freely accessible at the shrouded headers on the lower side of interface board. The digital outputs *DO28*...*DO31* are connected to four orange LEDs in the lower right corner of the board. The digital inputs *DI28*...*DI31* can be set via four sliding switches.

All other digital inputs and outputs from the RT Box are connected to the LaunchPad headers. To protect the inputs of the MCU from voltages greater than 3.3 V, the corresponding outputs of the RT Box are buffered with bus transceivers.

DO25 is connected to the MCU reset pin via the *RST* jumper. If the jumper is set a low-level output at DO25 will reset the MCU. Do not set this jumper unless you wish to use this feature.

Connectors

The following table contains the part numbers of the connectors and standoff assembly used on the LaunchPad interface board. For dimensions of the front panel of the RT Box, refer to the RT Box manual.

Sl. No.	Manufacturer	Part Number	Description
1	Sullins Connector Solutions	PRPC010DAAN-RC	20-pin Header
2	On Shore Technology Inc.	302-S161	16-pin Header
3	3M	961103-5604-AR	3-pin Header
4	3M	961102-6404-AR	2-pin Header
5	Radiall	R141426161	BNC Connector
6	Assmann WSW Components	A-DS 37 A/KG-T4S	37-pin D-Sub Male
7	Assmann WSW Components	ASUB-277-37TP25	37-pin D-Sub Stacked
8	Harwin Inc.	R6396-02	Hex Standoff
9	Keystone Electronics	720	Bumper
10	APM Hexseal	RM3X8MM 2701	M3 Screw

Table 2.3: Connectors and standoff assembly

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Appendix

The tables on the next pages provide more detailed information on the connectivity of the LaunchPad Interface. For each LaunchPad, the RT Box I/O is shown beside the header pins and the processor peripherals available at those pins. Note that only peripherals are listed which are compliant with the type and direction of the RT Box I/O.

LAUNCHXL-F28069M Pin Map

Function	RT Box			RT Box	Function
		J1	**J3**		
	3.3V	**1**	**21**		
		2	**22**	GND	
J1.3	DO0	**3**	**23**	AO0	ADCINA7
J1.4	DO1	**4**	**24**	AO1	ADCINB1
GPIO12, TZ1	DO2	**5**	**25**	AO2	ADCINA2
		6	**26**	AO3	ADCINB2
GPIO18, SPICLKA	DI24	**7**	**27**	AO4	ADCINA0
GPIO22, EQEP1S	DI25	**8**	**28**	AO5	ADCINB0
GPIO33, EPWMSYNCO, ADCSOCBO	DI26	**9**	**29**	AO6	ADCINA1
GPIO32, EPWMSYNCI	DO27	**10**	**30**	AO7	NC
		J5	**J7**		
	3.3V	**41**	**61**		
		42	**62**	GND	
J7.3	DO16	**43**	**63**	AO8	ADCINB7
J7.4	DO17	**44**	**64**	AO9	ADCINB4
GPIO20, EQEP1A	DO18	**45**	**65**	AO10	ADCINA5
		46	**66**	AO11	ADCINB5
		47	**67**	AO12	ADCINA3
GPIO21, EQEP1B	DO19	**48**	**68**	AO13	ADCINB3
		49	**69**	AO14	ADCINA4
		50	**70**	AO15	NC

Function	RT Box			RT Box	Function

Table 3.1: LAUNCHXL-F28069M pin map for J1, J3, J5 and J7

Function	RT Box			RT Box	Function
		J4	**J2**		
GPIO0, EPWM1A	DI0	**40**	**20**	GND	
GPIO1, EPWM1B	DI1	**39**	**19**	DI6	GPIO19, SPISTEA
GPIO2, EPWM2A	DI2	**38**	**18**	DI7	GPIO44, EPWM7B
GPIO3, EPWM2B	DI3	**37**	**17**		
GPIO4, EPWM3A	DI4	**36**	**16**	DO25	**RESET**
GPIO5, EPWM3B, SPISIMOA	DI5	**35**	**15**	DI27	GPIO16, SPISIMOA
GPIO13, TZ2, SPISOMIB	DO4	**34**	**14**	DO26	GPIO17, SPISOMIA, TZ3
NC	DO5	**33**	**13**	DO6	GPIO50, EQEP1A, TZ1
		32	**12**	DO7	GPIO51, EQEP1B, TZ2
		31	**11**	DO3	GPIO55, SPISOMIA, EQEP2B
		J8	**J6**		
GPIO6, EPWM4A, EPWM-SYNCO	DI16	**80**	**60**	GND	
GPIO7, EPWM4B	DI17	**79**	**59**	DI22	GPIO27, SPISTEB
GPIO8, EPWM5A, ADCSO-CAO	DI18	**78**	**58**	DI23	GPIO26, SPICLKB
GPIO9, EPWM5B	DI19	**77**	**57**		
GPIO10, EPWM6A, ADC-SOCBO	DI20	**76**	**56**		
GPIO11, EPWM6B	DI21	**75**	**55**	DO20	GPIO24, EQEP2A

Function	RT Box			RT Box	Function
		74	**54**	DO21	GPIO25, EQEP2B
		73	**53**	DO22	GPIO52, EQEP1S, TZ3
		72	**52**	DO23	GPIO53, EQEP1I
		71	**51**	DO24	GPIO56, EQEP2I

Table 3.2: LAUNCHXL-F28069M pin map for J2, J4, J6 and J8

LAUNCHXL-F28377S Pin Map

Function	RT Box			RT Box	Function
		J1	**J3**		
	3.3V	**1**	**21**		
		2	**22**	GND	
GPIO90	DO0	**3**	**23**	AO0	ADCIN14
GPIO89	DO1	**4**	**24**	AO1	ADCINB1
GPIO41	DO2	**5**	**25**	AO2	ADCINB4
		6	**26**	AO3	ADCINB2
GPIO60, SPICLKA, OUT-XBAR3	DI24	**7**	**27**	AO4	ADCINA0
GPIO61, SPISTEA, OUT-XBAR4	DI25	**8**	**28**	AO5	ADCINB0
GPIO43	DI26	**9**	**29**	AO6	ADCINA1
NC	DO27	**10**	**30**	AO7	NC
		J5	**J7**		
	3.3V	**41**	**61**		
		42	**62**	GND	
GPIO87	DO16	**43**	**63**	AO8	ADCIN15
GPIO86	DO17	**44**	**64**	AO9	ADCINA2
NC	DO18	**45**	**65**	AO10	ADCINA5
		46	**66**	AO11	ADCINB5
		47	**67**	AO12	ADCINA3
NC	DO19	**48**	**68**	AO13	ADCINB3
		49	**69**	AO14	ADCINA4

Function	RT Box			RT Box	Function
		50	**70**	AO15	NC

Table 3.3: LAUNCHXL-F28377 pin map for J1, J3, J5 and J7

Function	RT Box			RT Box	Function
		J4	**J2**		
GPIO12, EPWM7A	DI0	**40**	**20**	GND	
GPIO13, EPWM7B	DI1	**39**	**19**	DI6	GPIO4, EPWM3A, OUT-XBAR3
GPIO14, EPWM8A, OUT-XBAR3	DI2	**38**	**18**	DI7	GPIO62
GPIO15, EPWM8B, OUT-XBAR4	DI3	**37**	**17**		
GPIO16, EPWM9A, SPISI-MOA, OUTXBAR7	DI4	**36**	**16**	DO25	**RESET**
GPIO17, EPWM9B, OUT-XBAR8	DI5	**35**	**15**	DI27	GPIO58, SPICLKB, OUT-XBAR1, SPISIMOA
GPIO20, EQEP1A, SD1_D3	DO4	**34**	**14**	DO26	GPIO59, SD2_C2, SPISOMIA
GPIO21, EQEP1B, SD1_C3	DO5	**33**	**13**	DO6	GPIO72
		32	**12**	DO7	GPIO73
		31	**11**	DO3	GPIO78, EQEP2A
		J8	**J6**		
GPIO2, EPWM2A, OUT-XBAR1	DI16	**80**	**60**	GND	
GPIO3, EPWM2B, OUT-XBAR2	DI17	**79**	**59**	DI22	GPIO91
GPIO10, EPWM6A	DI18	**78**	**58**	DI23	NC

Function	RT Box			RT Box	Function
GPIO11, EPWM6B, OUT-XBAR7	DI19	**77**	**57**		
GPIO18, SPICLKA, EPWM10A	DI20	**76**	**56**		
GPIO19, SPISTEA, EPWM10B	DI21	**75**	**55**	DO20	GPIO63, EQEP3B, SD2_C4
		74	**54**	DO21	GPIO64, EQEP3S, SPISOMIB
		73	**53**	DO22	GPIO99, EQEP1I
		72	**52**	DO23	GPIO92
		71	**51**	DO24	NC

Table 3.4: LAUNCHXL-F28377 pin map for J2, J4, J6 and J8

LAUNCHXL-F28379D Pin Map

Function	RT Box			RT Box	Function
		J1	**J3**		
	3.3V	**1**	**21**		
		2	**22**	GND	
GPIO19, SD1_C2	DO0	**3**	**23**	AO0	ADCINA14, CMPIN4P
GPIO18, SD1_D2	DO1	**4**	**24**	AO1	ADCINC3, CMPIN6N
GPIO67	DO2	**5**	**25**	AO2	ADCINB3, CMPIN3N
		6	**26**	AO3	ADCINA3, CMPIN1N
GPIO60, SPICLKA, OUT-XBAR3, SPISIMOB	DI24	**7**	**27**	AO4	ADCINC2, CMPIN6P
GPIO22, EPWM12A, SPI-CLKB	DI25	**8**	**28**	AO5	ADCINB2, CMPIN3P
GPIO105	DI26	**9**	**29**	AO6	ADCINA2, CMPIN1P
GPIO104, EQEP3A	DO27	**10**	**30**	AO7	ADCINA0
		J5	**J7**		
	3.3V	**41**	**61**		
		42	**62**	GND	
GPIO139	DO16	**43**	**63**	AO8	ADCIN15, CMPIN4N
GPIO56, EQEP2S, SD2_D1	DO17	**44**	**64**	AO9	ADCINC5, CMPIN5N
GPIO97, EQEP1B	DO18	**45**	**65**	AO10	ADCINB5
		46	**66**	AO11	ADCINA5, CMPIN2N
		47	**67**	AO12	ADCINC4, CMPIN5P
GPIO52, EQEP1S, SD1_D3	DO19	**48**	**68**	AO13	ADCINB4
		49	**69**	AO14	ADCINA4, CMPIN2P

Function	RT Box			RT Box	Function
		50	**70**	AO15	ADCINA1

Table 3.5: LAUNCHXL-F28379D pin map for J1, J3, J5 and J7

Function	RT Box			RT Box	Function
		J4	**J2**		
GPIO0, EPWM1A	DI0	**40**	**20**	GND	
GPIO1, EPWM1B	DI1	**39**	**19**	DI6	GPIO61, SPISTEA, OUT-XBAR4
GPIO2, EPWM2A, OUT-XBAR1	DI2	**38**	**18**	DI7	GPIO123
GPIO3, EPWM2B, OUT-XBAR2	DI3	**37**	**17**		
GPIO4, EPWM3A, OUT-XBAR3	DI4	**36**	**16**	DO25	**RESET**
GPIO5, EPWM3B, OUT-XBAR3	DI5	**35**	**15**	DI27	GPIO58, SPICLKB, SPISI-MOA, OUTXBAR1
GPIO24, EQEP2A, SD2_D1	DO4	**34**	**14**	DO26	GPIO59, SPISOMIA, SD2_C2
GPIO16, SD1_D1	DO5	**33**	**13**	DO6	GPIO124, SD1_D2
		32	**12**	DO7	GPIO125, SD1_C2
		31	**11**	DO3	GPIO29, EQEP3B, SD2_C3
		J8	**J6**		
GPIO6, EPWM4A, OUT-XBAR4	DI16	**80**	**60**	GND	
GPIO7, EPWM4B, OUT-XBAR5	DI17	**79**	**59**	DI22	GPIO66, SPISTEB

Function	RT Box			RT Box	Function
GPIO8, EPWM5A, ADCSO-CAO	DI18	**78**	**58**	DI23	GPIO131
GPIO9, EPWM5B, OUT-XBAR6	DI19	**77**	**57**		
GPIO10, EPWM6A, ADC-SOCBO	DI20	**76**	**56**		
GPIO11, EPWM6B, OUT-XBAR 7	DI21	**75**	**55**	DO20	GPIO63, EQEP3B, SD2_C4
		74	**54**	DO21	GPIO64, EQEP3S, SPISOMIB
		73	**53**	DO22	GPIO26, EQEP2I, SD2_D2
		72	**52**	DO23	GPIO27, EQEP2S, SD2_C2
		71	**51**	DO24	GPIO25, EQEP2B, SPI-SOMIB, SD2_C1

Table 3.6: LAUNCHXL-F28379D pin map for J2, J4, J6 and J8

LAUNCHXL-F28027 Pin Map

Function	RT Box			RT Box	Function
		J4/J6	**J2/J2**		
GPIO0, EPWM1A	DI0	**40/1**	**20/1**	GND	
GPIO1, EPWM1B	DI1	**39/2**	**19/2**	DI6	GPIO19, SPISTEA
GPIO2, EPWM2A	DI2	**38/3**	**18/3**	DI7	GPIO12
GPIO3, EPWM2B	DI3	**37/4**	**17/4**		
GPIO4, EPWM3A	DI4	**36/5**	**16/5**	DO25	**RESET**
GPIO5, EPWM3B	DI5	**35/6**	**15/6**	DI27	GPIO16/32, SPISIMOA(16), ADCSOCA(32)
GPIO16/32, EPWM-SYNCI(32), TZ2(16)	DO4	**34/7**	**14/7**	DO26	GPIO17/33, SPISOMIA(17), TZ3(17)
GPIO17/33, SPISOMIA(17), TZ3(17)	DO5	**33/8**	**13/8**	DO6	GPIO6, EPWMSYNCI
		32/9	**12/9**	DO7	GPIO7
		31/10	**11/10**	DO3	NC
		J1	**J3/J5**		
	3.3V	**1**	**21/1**		
		2	**22/2**	GND	
GPIO28, TZ2	DO0	**3**	**23/3**	AO0	ADCINA7
GPIO29, TZ3	DO1	**4**	**24/4**	AO1	ADCINA3
GPIO34	DO2	**5**	**25/5**	AO2	ADCINA1
		6	**26/6**	AO3	ADCINA0
GPIO18, SPICLK	DI24	**7**	**27/7**	AO4	ADCINB1
	DI25	**8**	**28/8**	AO5	ADCINB3
	DI26	**9**	**29/9**	AO6	ADCINB7

	DO27	**10**	**30/10**	AO7	NC

Table 3.7: LAUNCHXL-F28027 pin map

LAUNCHXL-F280049C Pin Map

Function	RT Box			RT Box	Function
		J1	**J3**		
	3.3V	**1**	**21**		
		2	**22**	GND	
GPIO13	DO0	**3**	**23**	AO0	ADCINA5
GPIO40	DO1	**4**	**24**	AO1	ADCINB0
	DO2	**5**	**25**	AO2	ADCINC2
		6	**26**	AO3	ADCINB1
GPIO56, SPICLKA	DI24	**7**	**27**	AO4	ADCINB2
ADCINC4	DI25	**8**	**28**	AO5	ADCINC0
GPIO37, EQEP1B	DI26	**9**	**29**	AO6	ADCINA9
GPIO35, EQEP1A	DO27	**10**	**30**	AO7	ADCINA1
		J5	**J7**		
	3.3V	**41**	**61**		
		42	**62**	GND	
GPIO28, EQEP1A	DO16	**43**	**63**	AO8	ADCINA6
GPIO29, EQEP1B	DO17	**44**	**64**	AO9	ADCINB6
ADCINB4	DO18	**45**	**65**	AO10	ADCINC14
		46	**66**	AO11	ADCINC1
		47	**67**	AO12	ADCINC3
ADCINA8	DO19	**48**	**68**	AO13	ADCINC5
		49	**69**	AO14	ADCINA3
		50	**70**	AO15	ADCINA0

Table 3.8: LAUNCHXL-F280049C pin map for J1, J3, J5 and J7

Function	RT Box			RT Box	Function
		J4	**J2**		
GPIO10, EPWM6A, EQEP1A	DI0	**40**	**20**	GND	
GPIO11, EPWM6B, EQEP1B	DI1	**39**	**19**	DI6	GPIO57, SPISTEA
GPIO8, EPWM5A	DI2	**38**	**18**	DI7	
GPIO9, EPWM5B, EQEP1I, OUTXBAR6	DI3	**37**	**17**		
GPIO4, EPWM3A	DI4	**36**	**16**	DO25	**RESET**
GPIO5, EPWM3B, OUTXBAR3	DI5	**35**	**15**	DI27	GPIO16, SPISIMOA
GPIO58, OUTXBAR1	DO4	**34**	**14**	DO26	GPIO17, SPISOMIA
GPIO30, OUTXBAR7	DO5	**33**	**13**	DO6	GPIO39
		32	**12**	DO7	GPIO23
		31	**11**	DO3	GPIO59, EQEP1I
		J8	**J6**		
GPIO0, EPWM1A	DI16	**80**	**60**	GND	
GPIO1, EPWM1B	DI17	**79**	**59**	DI22	GPIO27, SPISTEB
GPIO6, EPWM4A	DI18	**78**	**58**	DI23	
GPIO7, EPWM4B, OUTXBAR5	DI19	**77**	**57**		
GPIO2, EPWM2A	DI20	**76**	**56**		
GPIO3, EPWM2B, OUTXBAR2	DI21	**75**	**55**	DO20	GPIO24, SPISIMOB
		74	**54**	DO21	GPIO31, SPISOMIB

Function	RT Box			RT Box	Function
		73	**53**	DO22	GPIO33, SPISTEB
		72	**52**	DO23	GPIO34
		71	**51**	DO24	GPIO12

Table 3.9: LAUNCHXL-F280049C pin map for J2, J4, J6 and J8

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