



PLECS

DEMO MODEL

Neutral-Point Clamped Converter

Last updated in PLECS 4.3.1

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The DC source, e.g., photovoltaic panels feeding a solar inverter, is modeled as a controlled current source. It provides 10 A_{DC} for the first half of the simulation and 15 A_{DC} for the second half of the simulation, corresponding to a sudden increase in received solar energy. This current charges the DC bus, which is split into two series-connected capacitors, with the mid-point connected to each of the three IGBT legs. Clamping diodes are placed between the capacitor mid-point and the one-quarter and three-quarter points of each leg. The mid-point of each leg is then fed to the respective phase of the AC grid via an inductor. The grid is modeled as an ideal three-phase 50 Hz, $130\text{ V}_{\text{RMS}}$ voltage source. The DC capacitors have initial voltages of 200 V_{DC} , though the setpoint for the DC bus is 450 V_{DC} , so they will charge up at the start of the simulation.

2.2 Controls

An outer voltage controller implemented as a PI regulator provides a current setpoint to an inner dq current controller. The voltage controller measures the DC voltage and calculates the error compared to the 450 V_{DC} reference value. The current controller has separate PI regulators for direct and quadrature currents that produce a V_{dq} reference. The AC phase voltages and currents are measured and fed to the current controller. A Phase-Locked Loop (PLL) generates the reference phase angle for the abc to dq transformations. A low pass filter is inserted into the feedback path from the $I_{\text{a,b,c}}$ measurement to represent the limited bandwidth of the current sensor. Modulation indices are generated for each of the three separate modulators for the three phase legs.

The three-level PWM modulator includes a simple neutral-point voltage balancing algorithm. One can look under mask of the “Symmetrical PWM (3-Level)” subsystem for the details. The “Vdc12” Signal In-port measures the upper and lower half DC voltages. The proportion of each regarding the ideal half DC voltage is calculated to proportionally move up (or down) the positive carrier (or the negative carrier), so that the modulated middle point voltage can change accordingly.

3 Simulation

Run the simulation with the model as provided to view the signals and observe that the DC voltage is regulated to 450 V_{DC} after the transients settle. The perturbation caused by the step change in current from the PV array is regulated out in approximately 50 ms. The switching pattern clearly shows a three-level pulse train with the fundamental waveforms phase-shifted. The real and reactive power delivered to the grid can also be observed.

Revision History:

PLECS 4.3.1 First release

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