



PLECS

*DEMO MODEL*

## Current Controlled Z-Source Inverter

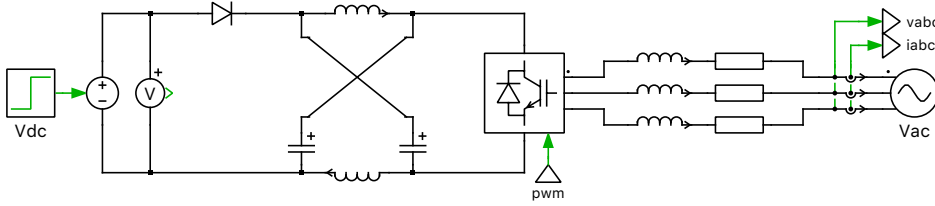
Last updated in PLECS 4.5.1

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# 1 Overview

This demonstration shows a current-controlled three-phase Z-source inverter used in a fuel-cell application. Fig. 1 shows the electrical circuit of the Z-source inverter. The unique impedance network in the Z-source inverter allows the inverter to be operated in both buck and boost modes.



**Figure 1: Electrical circuit of a Z-source inverter**

## 2 Model

The impedance-source (or impedance-fed) power converter, also abbreviated as Z-Source inverter (or converter) uses an impedance network, consisting of split-inductors and capacitors connected in an X shape, to couple the main converter circuit to the power source (or load). It can be used to implement DC-AC, AC-DC, AC-AC, and DC-DC power conversion, in place of traditional V-source or I-source converters.

The demo model shows an example of a Z-source inverter where a DC voltage from a fuel-cell source is converted into a three-phase AC output. A traditional V-source inverter (VSI) cannot produce an AC output voltage that is greater than the DC voltage without an additional DC-DC boost stage. A Z-source inverter can produce an AC output voltage that is both greater and less than the DC voltage depending on the buck-boost factor defined in section 2.1. A diode in series with the DC source is needed to prevent reverse current flow.

### 2.1 Operating Principle

In a traditional VSI, when the DC voltage is applied across the load, there are six active switching states possible (only one of the upper or lower switch conducts in each of the three phase legs), and two zero states (the load terminals are shorted either through all upper or all lower switches). The Z-source inverter has an additional zero state, when the load terminals are shorted through both the upper and lower switches of one or two or all three phase legs. This shoot-through zero state provides the unique buck-boost feature to the inverter. When the DC voltage is high enough to generate the desired AC voltage, the shoot-through zero state is inactive. Otherwise, the equivalent DC input voltage to the inverter is boosted using the shoot-through states [1].

For a symmetrical Z-source network, if the inverter bridge is in a shoot-through state for a period of  $T_0$ , and one of the eight non shoot-through states for a period of  $T_1$ , over one switching period of  $T$ ,

$$\frac{V_C}{V_{dc}} = \frac{T_1}{T_1 - T_0}$$

where,  $V_C$  is the average DC-link voltage across the inverter bridge and  $V_{dc}$  is the input voltage.

The peak DC-link voltage across the inverter bridge,  $\hat{v}_i$ , is:

$$\hat{v}_i = \frac{T}{T_1 - T_0} V_{dc} = B \cdot V_{dc}$$

where  $B$  is the boost factor resulting from the shoot-through zero state:

$$B = \frac{1}{1 - 2 \frac{T_0}{T}} \geq 1$$

The output AC peak phase voltage,  $\hat{v}_{ac}$ , from the inverter is:

$$\hat{v}_{ac} = M \cdot \frac{\hat{v}_i}{2} = M \cdot B \cdot \frac{V_{dc}}{2}$$

where,  $M$  is the modulation index.

The buck-boost factor,  $B_B$ , is calculated as:

$$B_B = M \cdot B = (0 \sim \infty)$$

The capacitor voltage,  $V_C$ , is calculated as:

$$V_C = \frac{1 - \frac{T_0}{T}}{1 - 2 \frac{T_0}{T}} V_{dc}$$

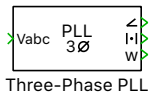
Therefore, shoot-through duty ratio,  $d$  is:

$$d = \frac{T_0}{T} = \frac{V_C - V_{dc}}{2 V_C - V_{dc}}$$

## 2.2 Controller

### Phase-Locked Loop

The PLECS component library offers a synchronous reference frame phase-locked loop (SRF-PLL) component, shown in Fig. 2. It contains a low-bandwidth proportional integral (PI) controller that detects the phase angle of the three-phase input signal. The phase information is then used to transform the AC output currents and voltages to a rotating reference frame (dq) [4].



**Figure 2: Synchronous reference frame phase-locked loop (SRF-PLL)**

### Current Controller

On the AC side, in the  $dq$  frame,

$$v_d = L \frac{d}{dt} i_d + R i_d + E_m - \omega L i_q$$

$$v_q = L \frac{d}{dt} i_q + R i_q + \omega L i_d$$

where,  $v_d$  and  $v_q$  are the voltages,  $i_d$  and  $i_q$  are the currents, and  $E_m$  is the peak value of phase A voltage. The cross-coupling terms  $\omega L i_q$  and  $\omega L i_d$  are a result of abc-to-dq transformation. In order to realize a simple first order plant, they are provided as a feed forward in the controller to decouple  $q$  and  $d$  axis currents.

With cancellation of cross-coupling terms, the plant transfer functions for the current controller in the  $dq$  frame are:

$$\frac{i_d(s)}{v_d(s)} = \frac{i_q(s)}{v_q(s)} = \frac{V_C/2}{sL + R}$$

The current controller is tuned analytically using the  $K$ -factor method, based on the above plant transfer functions. The  $K$ -factor method is a loop shaping technique, where a controller can be designed accurately for a specified phase margin and crossover frequency. Controller design using the  $K$ -factor method is explained in [2].

For a desired crossover frequency  $\omega_c$  of 1,000 Hz, the phase of the system is  $-89.95^\circ$ . If the desired phase margin is  $65^\circ$ , then the required phase boost ( $\phi_{\text{boost}}$ ) is  $64.95^\circ$ . Therefore, a type II controller is used. The transfer function of a Type II controller is:

$$G_c(s) = \frac{K_c}{s} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}$$

where  $K_c$  is the gain of the controller,  $\omega_z$  is the location of the zero and  $\omega_p$  is the location of the pole. The values of  $k$ ,  $\omega_z$  and  $\omega_p$  are calculated from the following expressions:

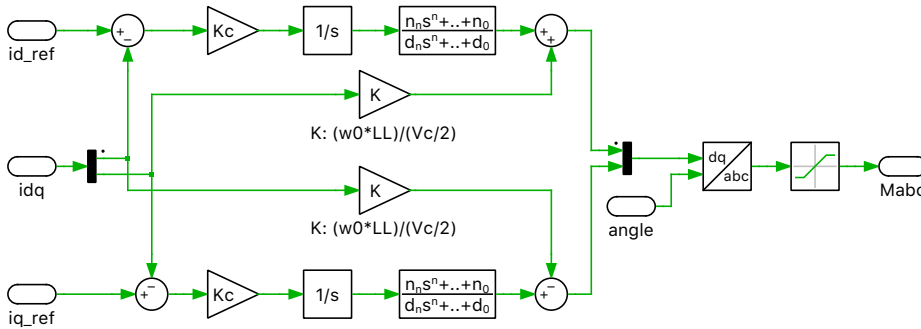
$$k = \tan \left( \frac{\phi_{\text{boost}}}{2} + 45^\circ \right); \omega_z = \frac{\omega_c}{k}; \omega_p = k \cdot \omega_z$$

$$\frac{1}{K_c} = \text{abs} \left( \frac{1}{j\omega_c} \cdot \frac{1 + \frac{1+j\omega_c}{\omega_z}}{1 + \frac{j\omega_c}{\omega_p}} \cdot G_p(j\omega_c) \right)$$

The value of  $K_c$  for the flyback converter is calculated as 502.

The output of the current controller is a three-phase set of sinusoidal signals  $\{M_a, M_b, M_c\}$ .

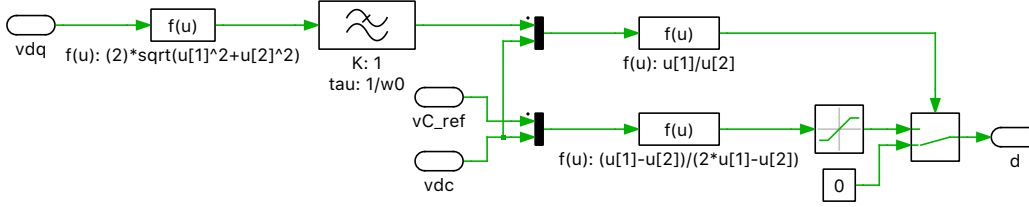
Fig. 3 shows the current controller implementation.



**Figure 3: Current controller**

### Shoot-through duty calculator

Whenever the buck-boost factor,  $B_B$  is greater than 1, the shoot-through duty ratio calculator calculates an open-loop shoot-through duty ratio,  $d$ , as shown in Fig. 4.



**Figure 4: Shoot-through duty calculator**

## 2.3 PWM Modulator

Shoot-through states are symmetrically inserted to existing pulse-width modulation (PWM) state patterns of a conventional VSI, as explained in [3]. For a three-phase set of sinusoidal signals  $\{M_a, M_b, M_c\}$  with  $M_{\max} = \max\{M_a, M_b, M_c\}$ ,  $M_{\text{mid}} = \text{mid}\{M_a, M_b, M_c\}$  and  $M_{\min} = \min\{M_a, M_b, M_c\}$ , shoot-through states are inserted as follows:

$$M_{\max}(SX) = M_{\max} + d$$

$$M_{\max}(SY) = M_{\max} + \frac{d}{3}$$

$$M_{\text{mid}}(SX) = M_{\text{mid}} + \frac{d}{3}$$

$$M_{\text{mid}}(SY) = M_{\text{mid}} - \frac{d}{3}$$

$$M_{\min}(SX) = M_{\min} - \frac{d}{3}$$

$$M_{\min}(SY) = M_{\min} - d$$

where,  $\{SX, SY\} = \{1, 2\}, \{3, 4\}$  or  $\{5, 6\}$  indicate switches 1 through 6 of the IGBT inverter.

A State Machine block is used to evaluate the above set of equations, as shown in Fig. 5. The PWM signals are then generated through carrier-based implementation using the newly calculated modulation indexes.

## 2.4 Simulation

Run the simulation with the model as provided to observe the PWM signals, output AC currents and Z-network capacitor voltage.

At 0.2 s, the d-axis AC current reference is increased from 5 A to 10 A, and at 0.4 s, the q-axis AC current reference is changed to -5 A. Observe that the output dq currents follow the reference signals, as shown in Fig. 6.

The output AC phase voltage is  $\frac{100}{\sqrt{3}}$  V and until 0.6 s, see Fig. 7, the input DC voltage is 70 V. Therefore, the buck-boost factor,  $B_B$ , is:

$$M \cdot B = \frac{2 \hat{v}_{ac}}{V_{dc}} = \frac{2 \cdot 100}{\sqrt{3} \cdot 70} = 1.65$$

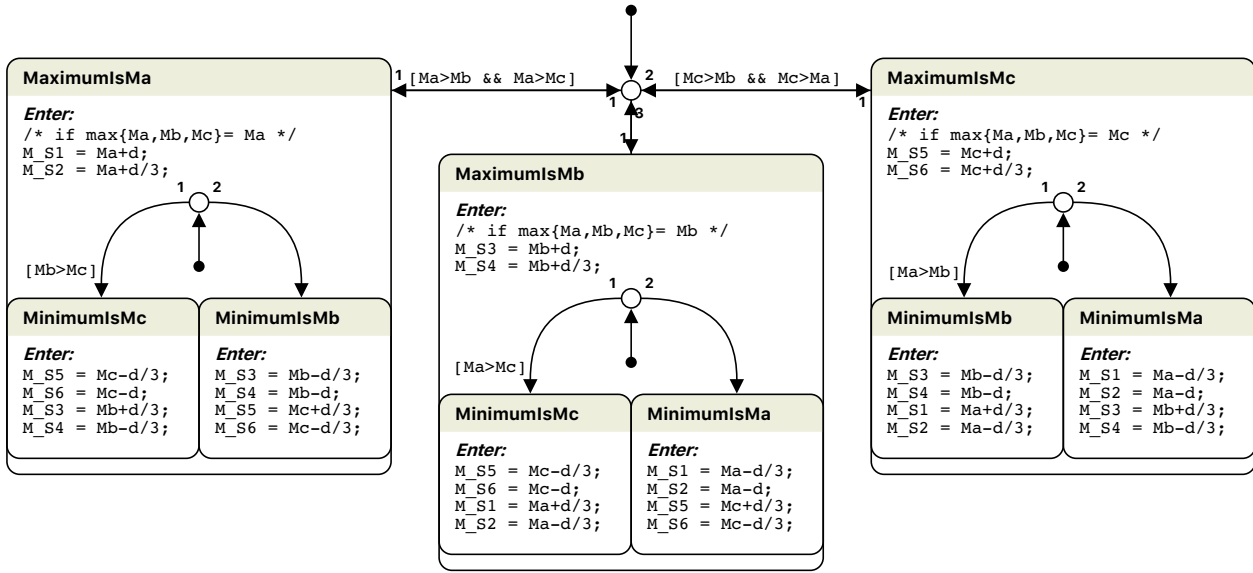


Figure 5: State machine modulator

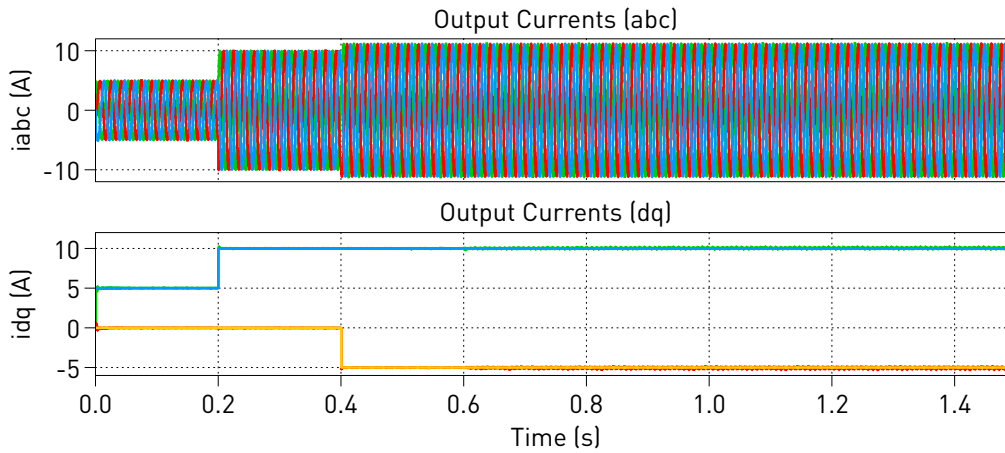


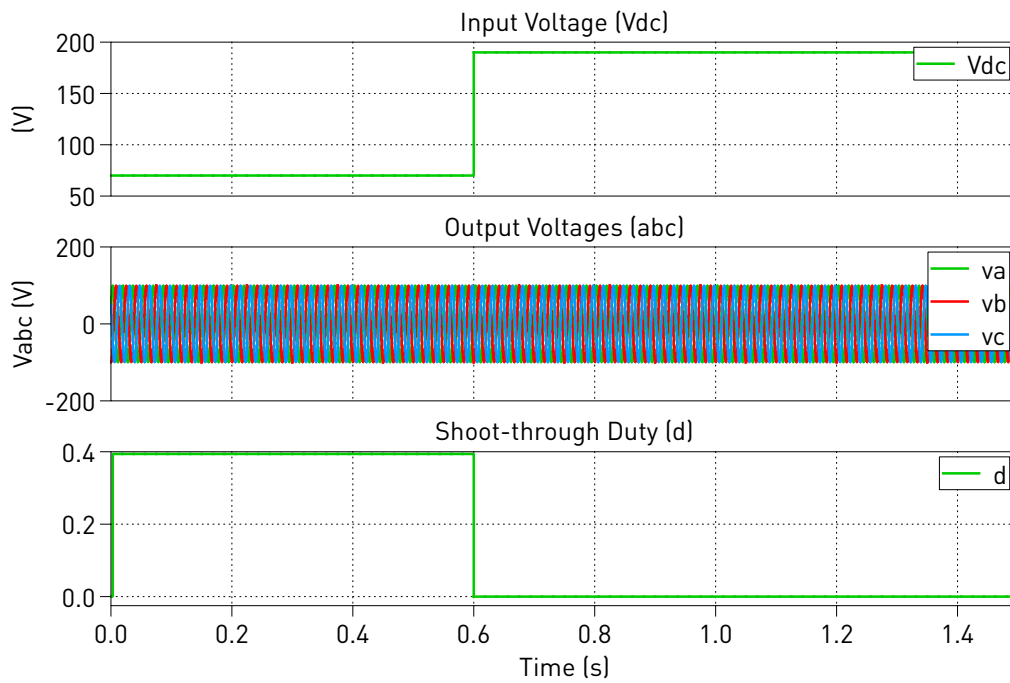
Figure 6: Output currents of the Z-Source inverter

Since the buck-boost factor is greater than 1, the shoot-through duty is enabled. The Z-source inverter operates in *Boost* mode. From Fig. 8, it can be observed that the shoot-through periods are symmetrically placed about the original switching instant.

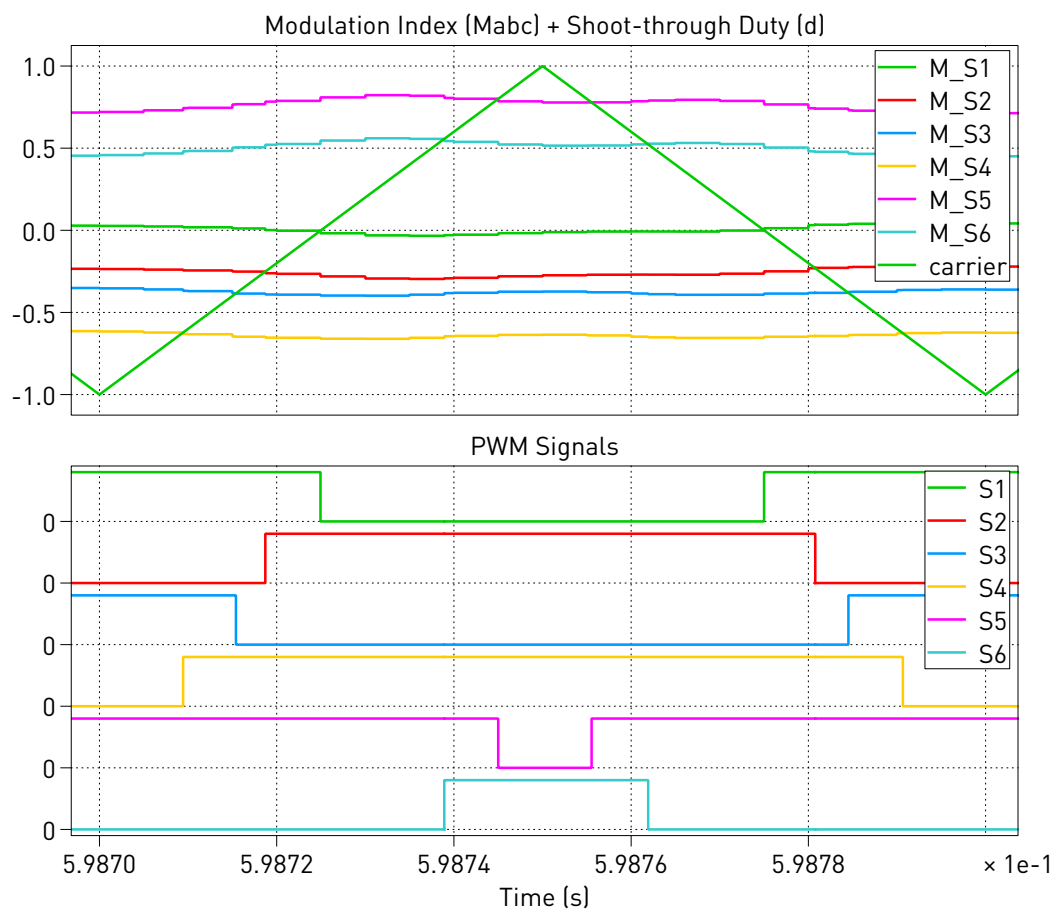
At 0.6 s, see Fig. 7, the input DC voltage is stepped up from 70 V to 190 V, and the new modulation index is calculated as:

$$M \cdot B = \frac{2 \hat{v}_{ac}}{V_{dc}} = \frac{2 \cdot 100}{\sqrt{3} \cdot 190} = 0.61$$

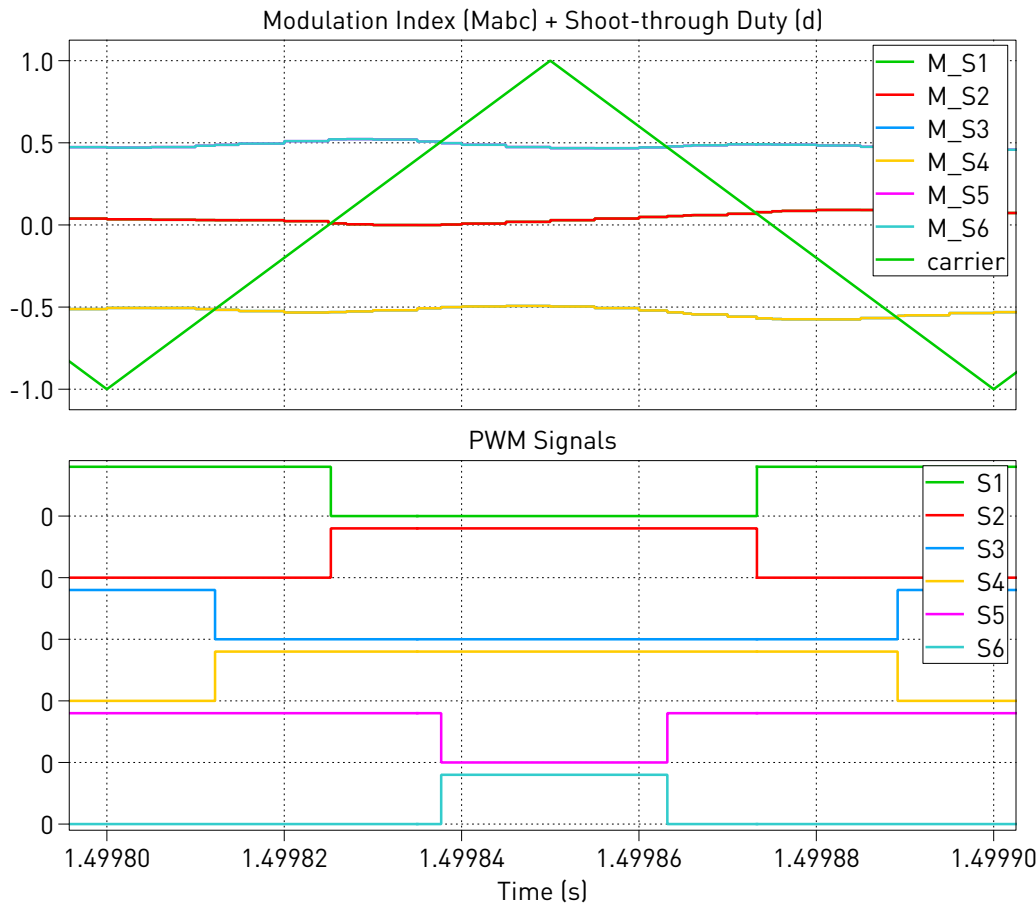
Since the buck-boost factor is less than 1, the shoot-through duty ratio is zero, as can be observed in Fig. 9. At this time, the Z-source inverter operates in *Buck* mode and the traditional PWM modulation scheme is used.



**Figure 7: Input and output voltages of the Z-Source inverter**



**Figure 8: PWM modulation of Z-source inverter with shoot-through enabled**



**Figure 9: PWM modulation of Z-source inverter with shoot-through disabled**

### 3 Conclusion

This model highlights a current-controlled, three-phase Z-source inverter, showcasing a few PLECS control domain components, including a continuous controller scheme and a state machine modulator. The State Machine block evaluates the maximum and minimum values of the three-phase sinusoidal modulation index signals generated by the current controller, and inserts the appropriate shoot-through duty value to obtain new compare signals.

### References

- [1] Fang Zheng Peng, "Z-source inverter," in *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504-510, March-April 2003. Click to access online: IEEE Xplore webpage.
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- [4] E. J. Bueno, F. J. Rodriguez, F. Espinosa and S. Cobrecas, "SPLL design to flux oriented of a VSC interface for wind power applications," in *31st Annual Conference of IEEE Industrial Electronics Society, 2005, IECON 2005.*, Raleigh, NC, 2005, pp. 6 pp. Click to access online: IEEE Xplore webpage.



## Revision History:

PLECS 4.3.1	First release
PLECS 4.5.1	Updating PLL component with new library block

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