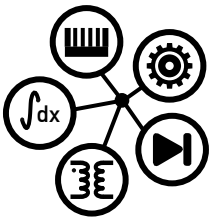

PLECS

DEMO MODEL

Bridgeless Boost PFC Converter

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1 Overview

This demonstration shows a single-phase AC/DC bridgeless power factor correction (PFC) boost rectifier circuit.

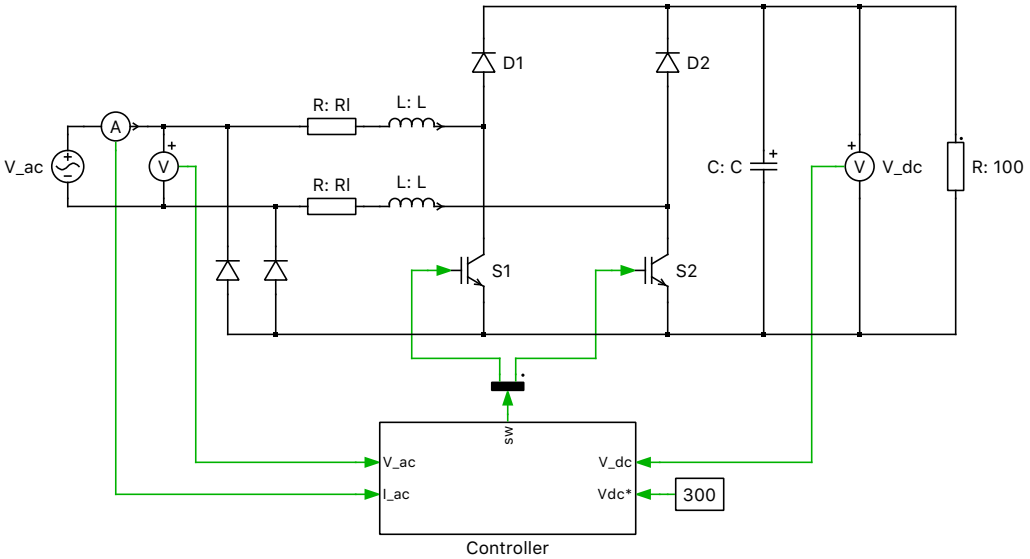

Fig. 1: Bridgeless boost PFC converter with Controller

Note

This model contains model initialization commands that are accessible from:
PLECS Standalone: the menu **Simulation > Simulation Parameters... > Initializations**
PLECS Blockset: right click in the **Simulink model window > Model Properties > Callbacks > InitFcn***

2 Model

2.1 Power circuit

The purpose of AC/DC PFC converters is to provide stable DC voltage output with low THD and high input power factor. A bridgeless PFC circuit is a combination of rectifier and boost converter. It can replace a conventional two-stage PFC circuit for higher converter efficiency. The schematic above shows a bridgeless PFC boost rectifier topology with two DC/DC boost circuits.

2.2 Circuit operation

The circuit operates in two switching half cycles of input AC line voltage. During the first half cycle, only one of the switches (S1 or S2) actively modulates, while the other switch stays on throughout the half cycle. During the second half cycle, they operate vice versa.

During the positive half cycle of the AC line voltage, switch S1 is actively modulating and switch S2 is continuously conducting. The circuit operation of the bridgeless PFC during the positive half cycle is shown in Fig. 2 and Fig. 3.

State 1: $V_{ac} > 0$, switch S1 is ON and switch S2 is ON. The mains current flows from the AC source through S1, S2 and D4. At the same time, the output capacitor discharges and supplies current to the load.

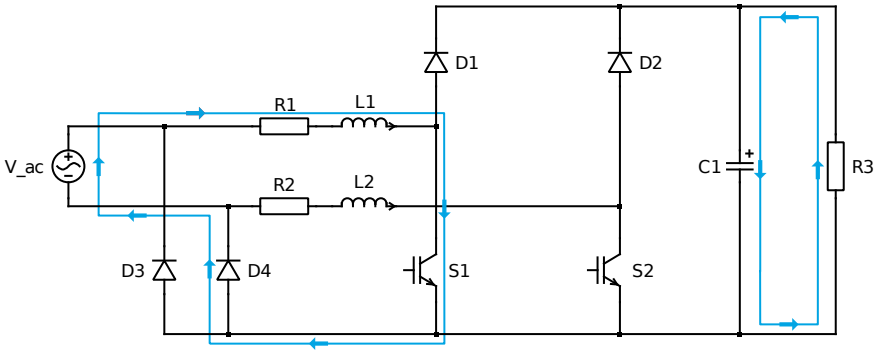

Fig. 2: Circuit operation for State 1, $V_{\text{ac}} > 0, S1 = ON, S2 = ON$

State 2: $V_{\text{ac}} > 0$, switch S1 is OFF and switch S2 is ON. The mains current flows through D1, the output capacitor, along with the load, S2 and D4.

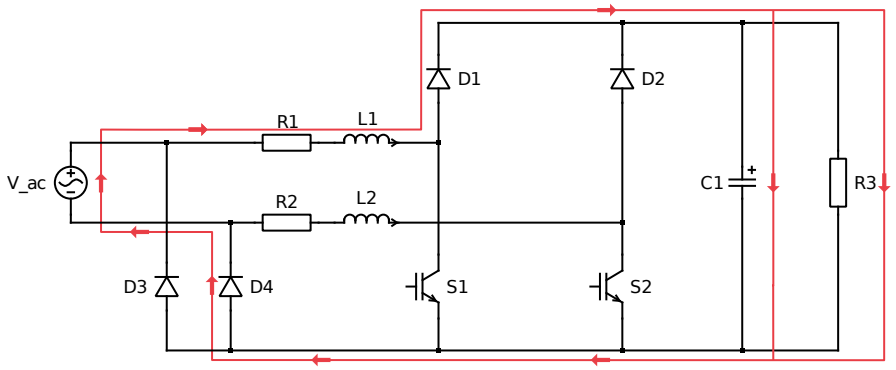

Fig. 3: Circuit operation for State 2, $V_{\text{ac}} > 0, S1 = OFF, S2 = ON$

During the negative half cycle of the input AC line voltage, switch S2 is actively modulating and switch S1 is continuously conducting. The circuit operation of the bridgeless PFC during the negative half cycle is shown in Fig. 4 and Fig. 5.

State 3: $V_{\text{ac}} < 0$, switch S1 is ON and switch S2 is ON. The mains current flows from the AC source through S2, S1 and D3. At the same time, the output capacitor discharges and supplies current to the load.

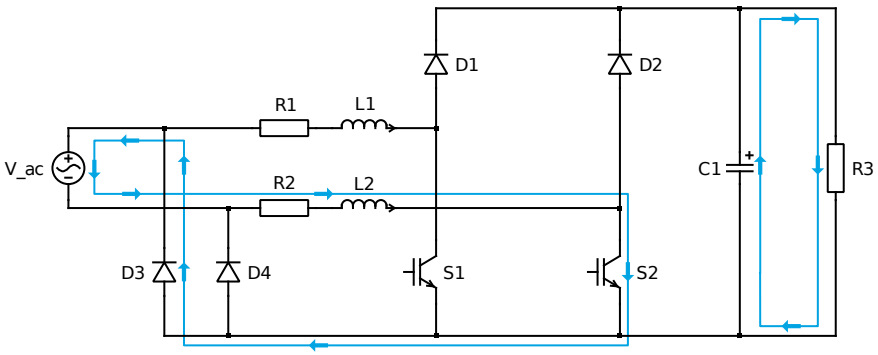

Fig. 4: Circuit operation fore State 3, $V_{\text{ac}} < 0, S1 = ON, S2 = ON$

State 4: $V_{\text{ac}} < 0$, switch S1 is ON and switch S2 is OFF. The mains current now flows through D2, the output capacitor, along with the load, S1 and D3.

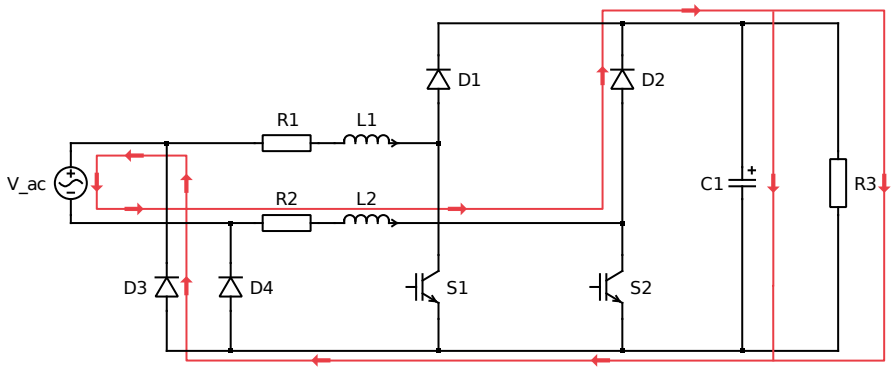

Fig. 5: Circuit operation for State 4, $V_{\text{ac}} < 0, S1 = ON, S2 = OFF$

2.3 Control

Fig. 6 depicts, the control scheme is composed of two loops - an outer voltage loop and an inner current loop. The error signal obtained by comparing the measured output voltage (DC) against a voltage set-point is given to the outer loop proportional-integral (PI) controller for voltage compensation. The voltage loop output is multiplied by the input voltage signal (AC) to generate the current reference. The inner loop proportional-resonant (PR) controller [2] controls the input current to follow the current reference. The resulting value is provided to a modulator for PWM generation. Logic is included in the controller such that the switches S1 and S2 either conduct or modulate throughout a half cycle based on the input voltage.

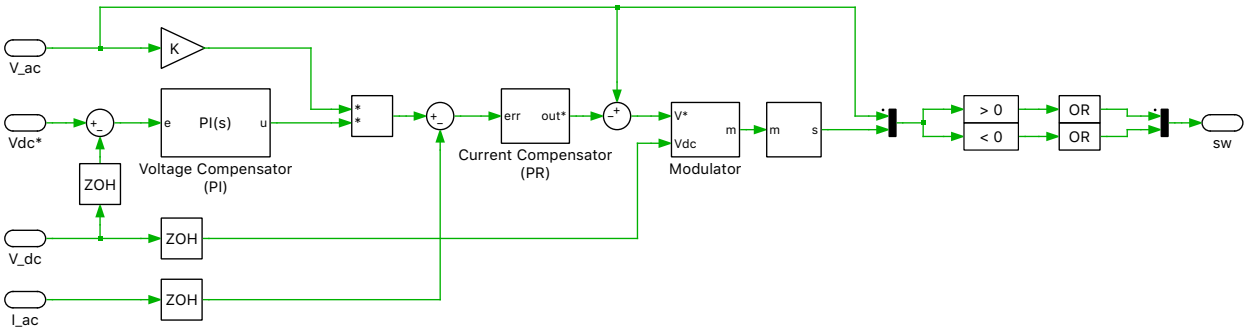

Fig. 6: Controller schematic

3 Simulation

Run the simulation to view output voltage, input current and scaled input voltage waveforms. Fig. 7 shows that the input voltage (in red) and the input current (in green) are almost in phase. At steady state, the ripple in the output voltage and the THD of the input current can be measured using the **Cursors** button at the top of the Scope.

From the **Drop-down** menu of the **Cursors** button select **Delta**, **Min**, **Max** and **THD**. Manually set the Delta value to the inverse of line frequency $(1/F)$. The data table then displays the value for the minimum, maximum, and the THD of the signal between the cursors. The resulting output voltage ripple is $8.9\,\%$ and the THD of the input current is $6.2\,\%$. The distortion power factor associated with the input current is 0.9981. The harmonic order of these waveforms can also be viewed using the **Fourier spectrum** button at the top of the Scope.

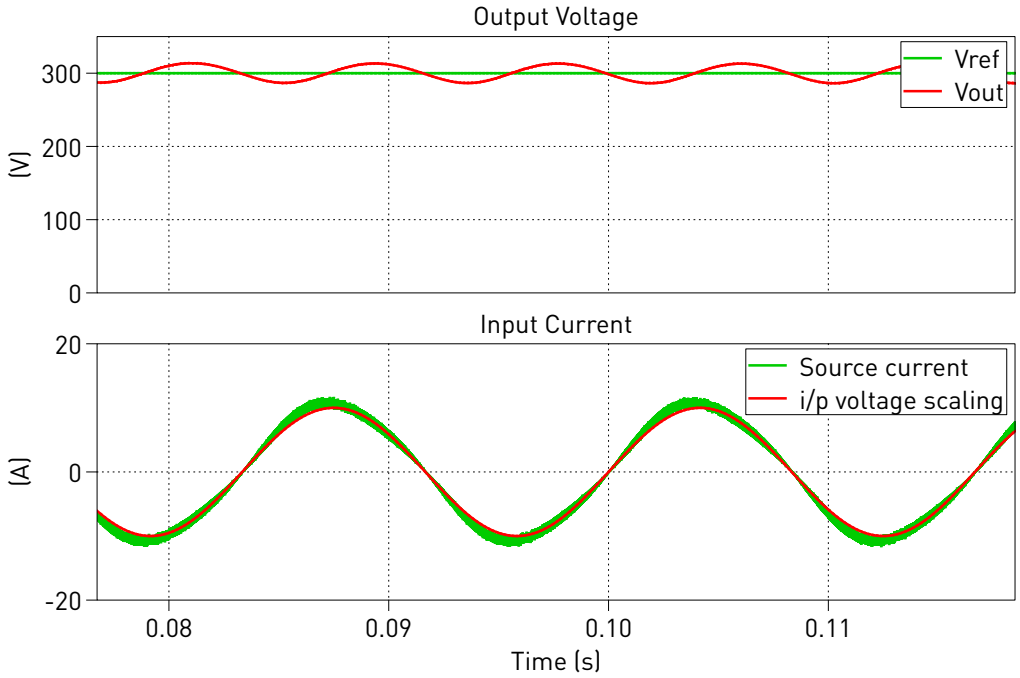

Fig. 7: Comparison of input current and scaled input voltage in steady state

4 Bibliography

[1] L. Huber, Y. Jang and M. M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers" in IEEE Transactions on Power Electronics, vol. 23, no. 3, pp. 1381-1390, May 2008.

[2] R. Teodorescu, F. Blaabjerg, "Proportional-Resonant Controllers. A New Breed of Controllers Suitable for Grid-Connected Voltage-Source Converters," in Journal of Electrical Engineering.

Revision History:

PLECS 4.3.1	First release
PLECS 4.4.2	Update PI controller component

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PLECS Demo Model