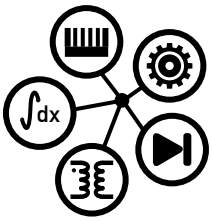

PLECS

DEMO MODEL

Buck Converter with Peak Current Control

Last updated in PLECS 4.3.1

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1 Overview

This demonstration shows a current-controlled buck converter with a resistive load. The PLECS Peak Current Controller block is used to implement peak current mode control and a voltage control loop is provided in both analog and digital implementations.

2 Model

2.1 Power circuit

A simple buck converter topology is used to produce $12\,\mathrm{V}$ from a $24\,\mathrm{V}$ source and demonstrates an output power between ~ 25 and $75\,\mathrm{W}$.

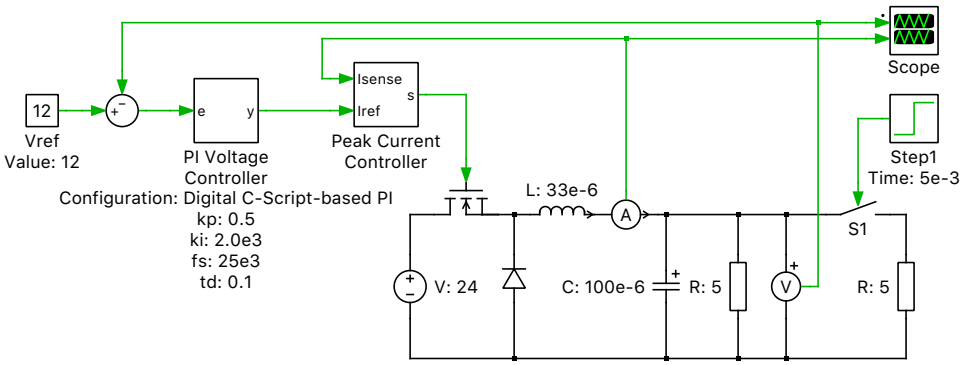

Fig. 1: Buck Converter with Peak Current Control

2.2 Control

The switch modulation is generated by the PLECS Peak Current Controller block. This controls the peak current flowing through the inductor. Slope compensation is used to ensure stability when the duty cycle exceeds $50\,\%$. An outer voltage control loop supplies the reference current for the peak current mode control and this is implemented using a masked configurable subsystem. The subsystem contains both a discrete and continuous PI voltage control implementation. By looking under the mask (**Ctrl+U**, on macOS: **Cmd+U**) of the PI Voltage Controller block, the two control implementations can be viewed.

The digital PI controller implementation includes an optional calculation delay. In a practical system, a finite delay exists due to the time needed for the controller to read the input(s), perform the control calculation and write to the output(s), and can degrade the stability for certain systems. The parameters for the proportional and integrator gains, as well as the sampling frequency and calculation delay are masked parameters for the controller subsystem. Since they are directly passed to the C-Script block as inputs, the values can be changed at the top level of the schematic for analyzing various effects. Note that for the analog implementation the subsystem mask parameters for switching frequency and calculation delay are not relevant.

3 Simulation

The simulation demonstrates the start-up of the converter and a load step half way through the simulation. When the load resistance is halved, the current doubles and the perturbation in the voltage is regulated out in approximately $200\,\mu\mathrm{s}$.

The voltage control scheme can be toggled between analog and digital implementations. To observe the influence of the calculation delay in the digital voltage controller implementation, set the switching frequency to $10\,\mathrm{kHz}$ and run the simulation for a calculation delay of 0.1 and 0.9.

Revision History:

PLECS 4.3.1	First release

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PLECS Demo Model

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