PLECS

DEMO MODEL

Flying Capacitor DC-DC Converter

Last updated in PLECS 4.8.1

1 Overview

This demonstration illustrates a flying capacitor (FC) DC/DC converter (also known as a multicell, imbricated cell or switched-capacitor converter), which is a type of multilevel converter. FC converters comprise solely switches and capacitors in the switching cell. This model is designed to step down the input voltage to an output voltage that can be configured by adjusting the duty cycle of the modulator.

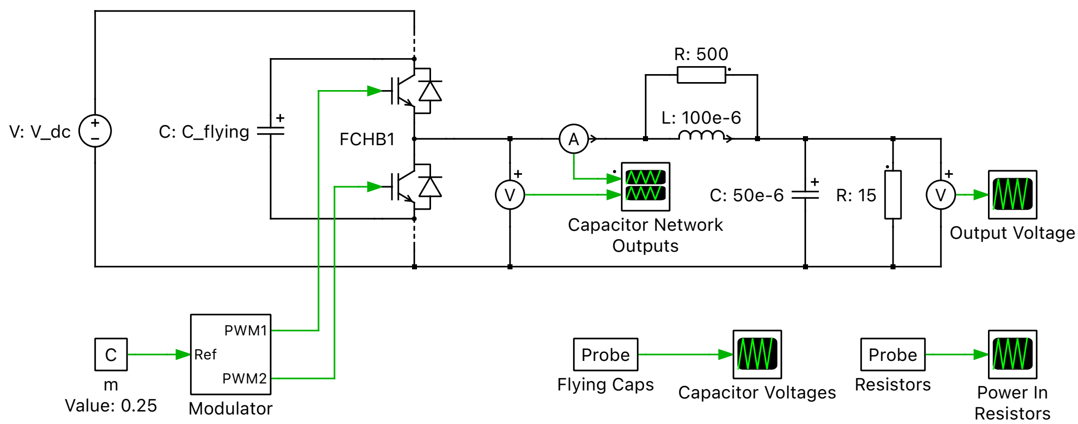

Fig. 1: Flying capacitor DC/DC converter

> **Note**
>
> This model contains model initialization commands that are accessible from:
> *PLECS Standalone:* the menu **Simulation > Simulation Parameters... > Initializations**
> *PLECS Blockset:* right click in the **Simulink model window > Model Properties > Callbacks > InitFcn***

2 Model

2.1 Power circuit

The circuit is modeled as a modular multilevel multicell network, where each cell contains two switches connected by a clamping capacitor. The switch pair and capacitors are connected in series to form a chopper circuit network. A DC voltage source powers the input and generates an AC or DC quantity at the output of the switch capacitor network, depending on the reference duty cycle of the modulator. The generic configurable-length multicell network is shown in Fig. 2.

The Flying Capacitor Half Bridge module in PLECS is implemented using a modular subsystem concept, where a dynamically-sized chain of components is connected using wires and multiplexers. This module implementation is depicted in Fig. 3 on p. 4. The input and output of the module are configured as the terminals of the flying capacitor chain. The commutation cell is repeated by means of routing its output back into its input $n-1$ times, for a user-specified number of cells n. As shown below, the trick to this implementation is defining one of the wires in each multiplexer to have a width of $n-1$. By using a wired loop, this creates a chain with the components in between the multiplexers (a switch pair and clamping capacitor) being replicated in a series-connected fashion n times.

The capacitor connected to this module is in a vectorized fashion. The balanced chopped capacitor voltage levels are $(n-1)V_{\mathrm{dc}}/n, \ldots, 2 \cdot V_{\mathrm{dc}}/n, V_{\mathrm{dc}}/n$, ordered from outer to inner level.

Since the input is $600\,\mathrm{VDC}$ and $n = 3$, the two capacitor voltage levels are 400 and $200\,\mathrm{VDC}$. The output of the capacitor network has significant ripple and needs to be filtered before the load. An LC low pass

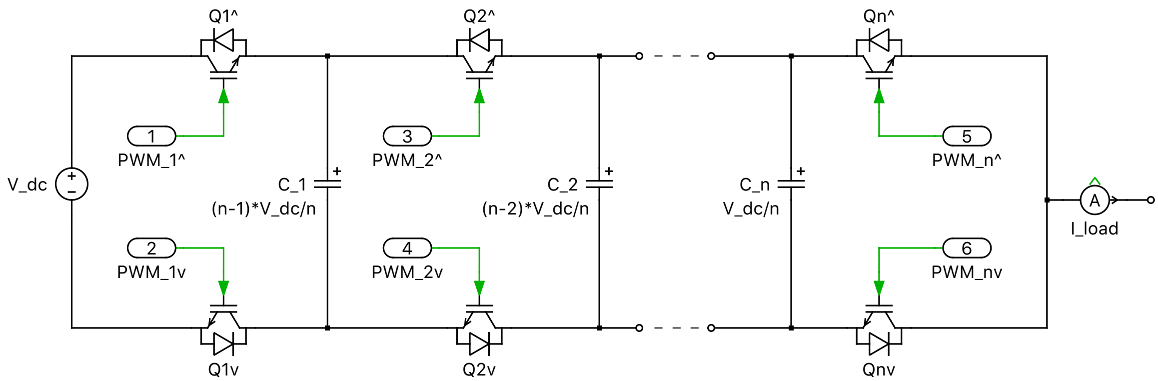

Fig. 2: Configurable-length multicell network

filter is used for this purpose. A voltage booster is also included in parallel to the inductor, which helps to speed up the balancing of the system during transients [1].

2.2 Control

The modulation scheme is a phase-shifted carrier pulse-width modulation (PSCPWM) technique using a fixed duty cycle. There are n triangular carriers, each shifted from the previous one by $2\pi/n$. The controller provides two pulse-width modulated signals that gate the upper and lower IGBTs with the same duty cycle in a complementary fashion. A dead time is included to delay the turn-on between switch commutation for each switch pair. The converter doesn't require closed-loop control because the capacitors themselves will self-balance as each commutation cell has equal duty cycles and $2\pi/n$ phase shifts, as discussed in [2]. Any changes to the DC input or having unbalanced initial capacitor voltages will produce a transient, but the system will settle to a well-defined steady-state operating point without feedback regulation.

3 Simulation

Run the simulation with the model as provided to view the signals and verify that the load settles at $V_{\mathrm{dc}} \cdot D = 600\,\mathrm{V} \cdot 0.25$, or approximately $150\,\mathrm{VDC}$. In fact, the voltage at the load is slightly less due to deadtime and non-ideality of the output network. The output voltage can be adjusted by changing the duty cycle reference at the Constant block that is fed into the Modulator subsystem. Also, the number of cells in the network can be changed in the model initialization commands. The self-balancing nature of the capacitor network is shown with the transient behavior of the waveforms in the "Capacitor Voltages" Scope. Two capacitor voltages when $n = 3$ are depicted in Fig. 4. By providing an initial voltage to the capacitors ($500\,\mathrm{VDC}$) that is different than the DC bus ($600\,\mathrm{VDC}$), the capacitor voltages will migrate towards stacked DC levels of V_{dc}/n and the cell voltages will all balance each other at $V_{\mathrm{dc}}/n = 200\,\mathrm{VDC}$.

4 Bibliography

[1] T. A. Meynard, H. Foch, P. Thomas, et al, "Multicell converters: Basic concepts and industry applications", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 955-964, Oct. 2002.

[2] R. H. Wilkinson, T. A. Meynard, and H. du T. Mouton, "Natural balance of multicell converters: The general case", *IEEE Transactions on Power Electronics*, vol. 21, pp. 1658-1666, Nov. 2006.

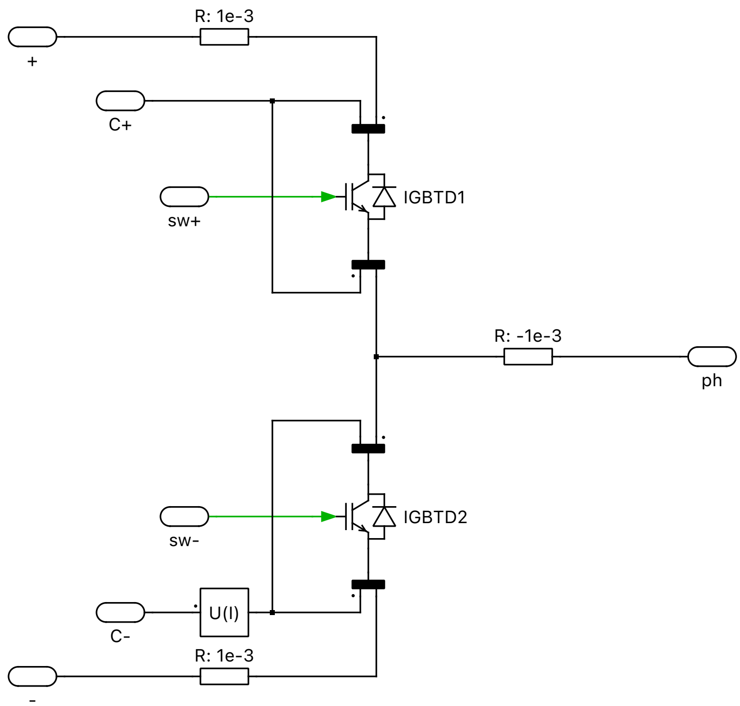

Fig. 3: Cell implementation of flying capacitor DC/DC converter

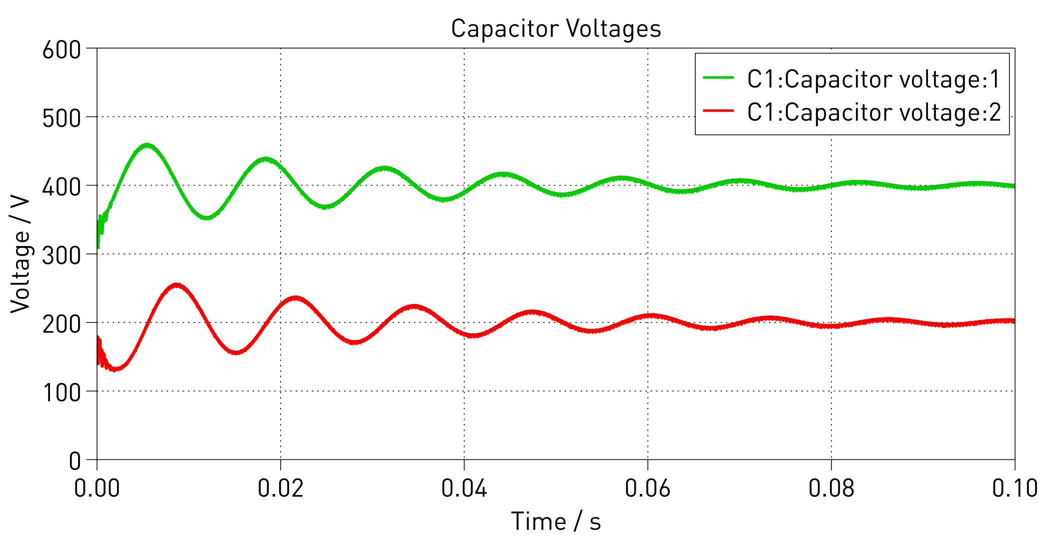

Fig. 4: Simulation result of capacitor voltages at different cell output

Revision History:

PLECS 4.3.1	First release
PLECS 4.8.1	Use the Flying Capacitor Half Bridge power module from the library

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