PLECS

DEMO MODEL

Three-Phase Diode Bridge Rectifier

Last updated in PLECS 4.8.1

1 Overview

This example shows a three-phase, full-wave diode bridge rectifier with a configurable capacitive or inductive load. Three-phase rectifiers, also known as six-pulse rectifiers, are common in industrial and high-power applications.

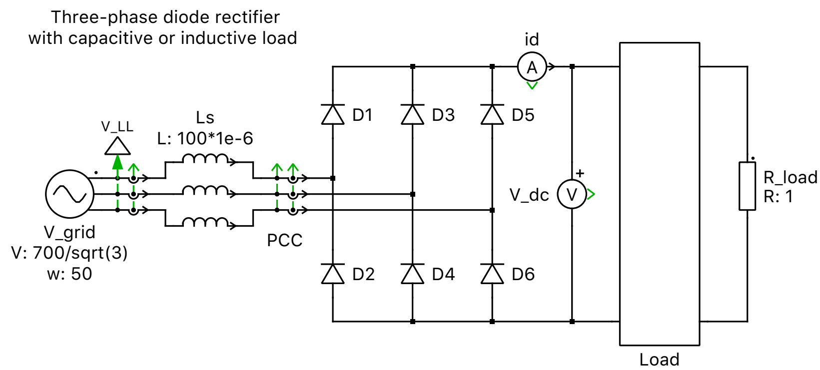

Fig. 1: Three phase diode rectifier

2 Electrical model

A diode rectifier is used for AC/DC conversion and allows the flow of current only in the direction of AC-input to DC-output. A full-wave rectifier converts a sinusoidal input waveform into positive half sinusoidal waves at twice the input frequency. In the case of a single-phase rectifier, the output voltage waveform is the absolute magnitude of the AC input voltage. For a bridge rectifier drawing three-phase balanced currents, however, the resulting output voltage on the DC side will show six pulses per cycle of the grid frequency.

2.1 Output Voltage

The average output voltage for a six-pulse rectifier without grid-side inductance ($L_s = 0$) and capacitive load is calculated as:

$$V_{\mathrm{dc}} = \frac{3 \cdot \hat{V}_{\mathrm{LL}}}{\pi}$$

where $\hat{V}_{\mathrm{LL}}$ is the amplitude of the line-to-line AC voltage.

The grid side inductance makes the current commutate between the diodes over a finite time interval. Due to this effect the average output voltage is reduced if $L_s > 0$. The formula for V_{dc} changes to [1]:

$$V_{\mathrm{dc}} = \frac{3}{\pi}\left(\hat{V}_{\mathrm{LL}} - \omega L_s \bar{i}_d\right)$$

paragraph{Load} The load for the rectifier system is implemented as a configurable subsystem, with choices for either a capacitive or inductive load. Note that with a capacitive load the DC and load voltages are the same, and with an inductive load the DC and load currents are the same.

3 Simulation

- Run a simulation with the default line inductance $L_s = 100\,\mu\mathrm{H}$ and observe the commutation interval in the rectifier input voltage. During the commutation interval the rectifier input voltage stays zero which leads to a lower average V_{dc}. This can be seen in Fig. 2 that shows the different system quantities for line inductance values of $L_s = \{0, 30, 100\}\,\mu\mathrm{H}$.

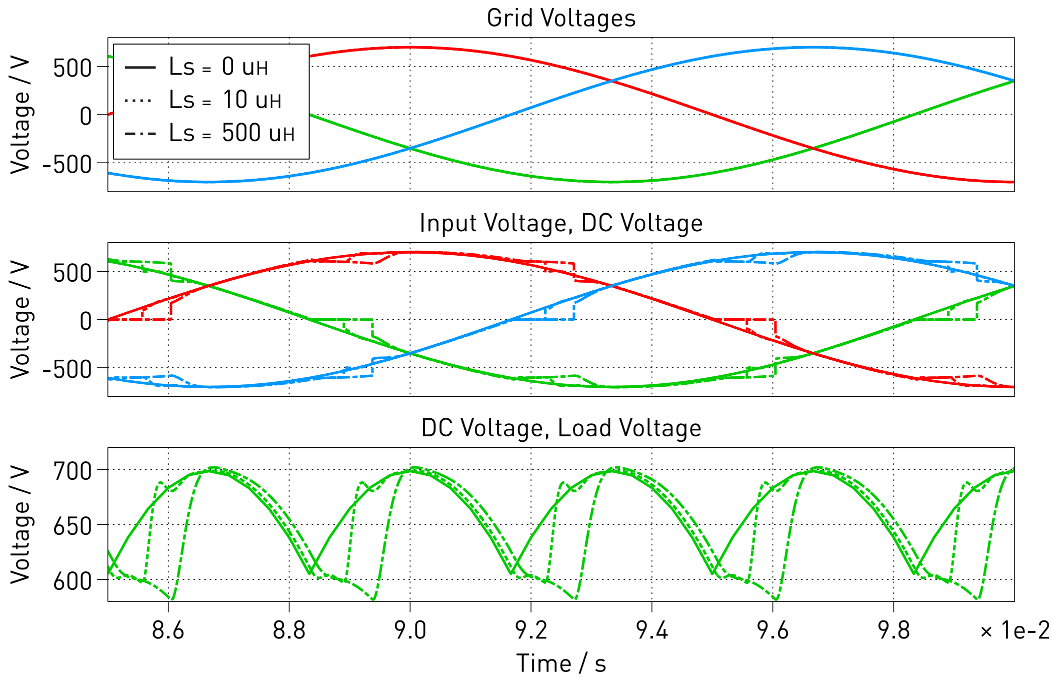

Fig. 2: Results of the simulation showing the commutation interval for a finite line inductance

- Tune the load parameters and observe the resulting DC-side waveforms. Check that a larger load inductance reduces the DC voltage ripple, for example. Keep in mind that the waveforms will only reflect a change in the load parameters if that respective load type is active (changing the capacitance value when the inductive load subsystem configuration is active will not have any influence on the simulated results).

4 Bibliography

[1] N.Mohan, T.M. Undeland, W.P. Robbins, *Power Electronics: Converters, Applications, and Design*, John Wiley & Sons, 2003

Revision History:

PLECS 4.3.1	First release
PLECS 4.8.1	Add information about commutation interval

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