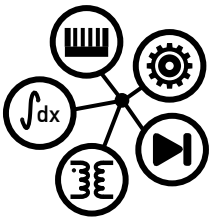

PLECS

DEMO MODEL

Two Stage LED driver

Last updated in PLECS 4.3.1

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1 Overview

This demonstration shows the design of a two-stage LED driver circuit consisting of a boost-PFC for AC/DC conversion followed by a flyback converter for DC/DC conversion.

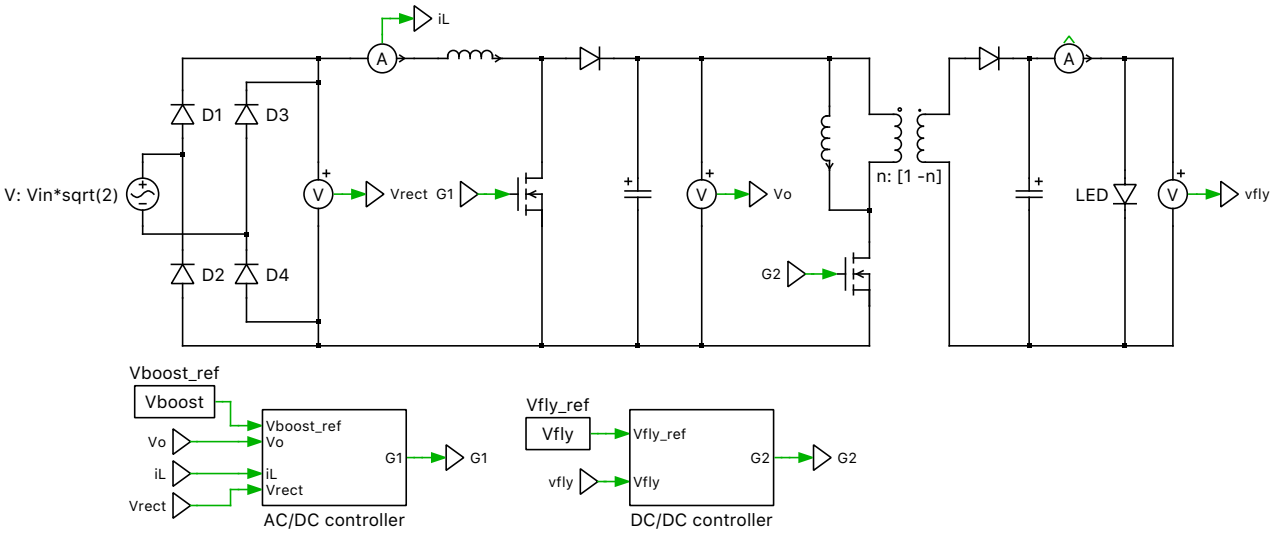

Fig. 1: Two-stage LED Driver with controller

Note

This model contains model initialization commands that are accessible from:
PLECS Standalone: the menu **Simulation > Simulation Parameters... > Initializations**
PLECS Blockset: right click in the **Simulink model window > Model Properties > Callbacks > InitFcn***

2 Model

2.1 Power Circuit

For LED drivers in general lighting applications, the induced line current harmonics must comply with IEEE Std 519-2014. Generally, it is difficult to meet these requirements without power factor correction (PFC) techniques. In the two-stage LED driver circuit designed in this model, the first stage provides a near unity power factor and a low total harmonic distortion (THD), while the second DC/DC stage is used to provide a tight regulation of the output. The Boost PFC converter attempts to draw a current that is always in phase with and at the same fundamental frequency as the line voltage, while maintaining a constant DC bus voltage on its output.

The LED load is represented by a non-linear V-I curve obtained from the forward current characteristic curve (forward voltage vs forward current) provided in the data sheet [1] . For the LEDs considered in this model, the typical forward voltage is $3.2\,\mathrm{V}$ and typical forward current is $35\,\mathrm{mA}$; ten of these LEDs are connected in series to form a “light engine”.

2.2 Controller

The two-stage LED driver requires two independently controlled power switches and two control circuits for AC/DC and DC/DC conversion.

The AC/DC controller comprises of an inner current loop that operates faster than the outer voltage loop. The voltage compensator regulates the DC output voltage, by comparing the sensed DC output signal against a reference. The output of the voltage loop is proportional to the amount of power transferred by the PFC converter. This output is then multiplied by the rectified input voltage and the inverse of the square of the RMS input voltage, implementing fast feed-forward control. This modulates the voltage controller output such that the PFC input current and the PFC input voltage have the same phase. The resulting product is compared against the sensed PFC rectified input current. This error is the input to the current loop. The current controller generates the PFC duty ratio command such that the PFC input current tracks the reference current.

The DC/DC controller is used for voltage regulation. The error signal obtained by comparing the measured output voltage (DC) against a voltage setpoint is given to the controller for voltage compensation. The resulting value is provided to a modulator for PWM generation.

The controllers in both these cases have been tuned analytically using the K-factor method, based on the respective plant transfer functions of the converters. The K-factor method is a loop shaping technique, where a controller can be designed accurately for a specified phase margin and crossover frequency. Controller design using the K-factor method is explained in Dr. Raja Ayyanar's videos on K-factor controller design [2].

For example, the K-factor method implementation for the DC/DC converter is shown below.

The flyback converter output voltage-to-duty transfer function, using a worst case duty ratio of 0.5 and with the inductance reflected to the secondary side, is:

$$G_{\mathrm{p}}(s) = \frac{16 \cdot V_{\mathrm{out}} \cdot (0.5 \cdot R - sL)}{R + 4 \cdot sL + 4 \cdot s^2 RLC}$$

For a desired crossover frequency ω_c of $300\,\mathrm{Hz}$, the phase of the system is $-33.2°$. If the desired phase margin is $60°$, then the required phase boost (ϕ_{boost}) is $3.2°$. Therefore, a type II controller is used. The transfer function of a Type II controller is:

$$G_{\mathrm{c}}(s) = \frac{K_{\mathrm{c}}}{s} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}$$

where K_{c} is the gain of the controller, ω_z is the location of the zero and ω_p is the location of the pole. The values of k, ω_z and ω_p are calculated from the following expressions:

$$k = \tan\left(\frac{\phi_{\mathrm{boost}}}{2} + 45°\right);\ \omega_z = \frac{\omega_z}{k};\ \omega_p = k \cdot \omega_z$$

$$\frac{1}{K_c} = \mathrm{abs}\left(\frac{1}{j\omega_c} \cdot \frac{1 + \frac{1 + j\omega_c}{\omega_z}}{1 + \frac{J\omega_c}{\omega_p}} \cdot G_p(j\omega_c)\right)$$

The value of K_{c} for the flyback converter is calculated as 2.7094.

3 Simulation

Run the simulation with the model as provided to view the input and the output signals. At steady state, the ripple in the output voltage, output current and the THD of the input current can be measured using the **Cursors** button at the top of the scope.

In the scope labeled Inputs, from the **Drop-down** menu of the **Cursors** button select **Delta** and **THD**. Manually set the Delta value to the inverse of line frequency $(1/F)$. The data table then displays the value for the THD of the signal between the cursors. The resulting THD of the input current is $4.7\,\%$. The distortion power factor associated with the input current is 0.999, as calculated by:

$$DPF = \frac{1}{\sqrt{1 + THD^2}} = \frac{1}{\sqrt{1 + 0.047^2}}$$

In the scope labeled Outputs, select **Max**, **Min** and {Mean} from the **Drop-down** menu of the **Cursor** button. The resulting output peak-to-peak current ripple ($Io_{\mathrm{pk-pk}}$) is $10.3\,\%$.

$$Io_{\mathrm{pk-pk}} = \frac{Io_{\max} - Io_{\min}}{Io_{\mathrm{avg}}} \cdot 100\,\% = 10.3\,\%$$

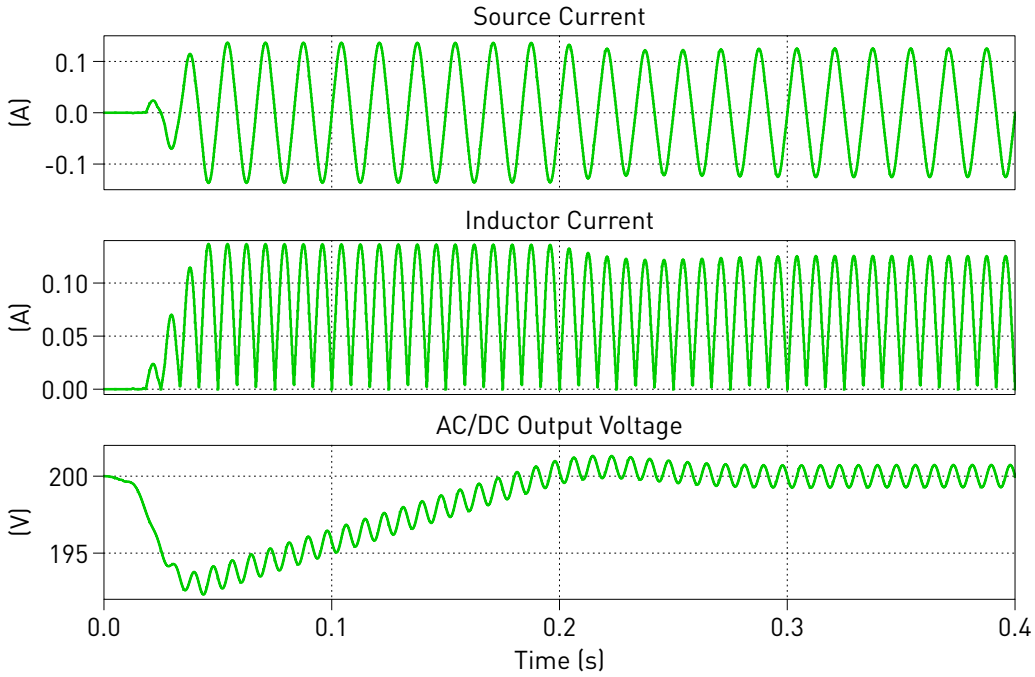

Fig. 2: Simulation result input

The harmonic order of these waveforms can also be viewed using the **Fourier spectrum** button at the top of the scope.

4 Bibliography

[1] Datasheet for “Golden DRAGON, LW W5SM”. Click to access online: Osram LW W5SM datasheet[1].

[2] Videos on K-factor controller design by Dr. Raja Ayyanar. Click to access online:

- k-factor control design method: part 1[2]
- k-factor control design method for dc dc part2[3]

[1] https://dammedia.osram.info/media/resource/hires/osram-dam-5231534/LW%20W5SM_EN.pdf
[2] https://www.youtube.com/watch?v=ExFV-CPevmU
[3] https://www.youtube.com/watch?v=RmREot5DUtk

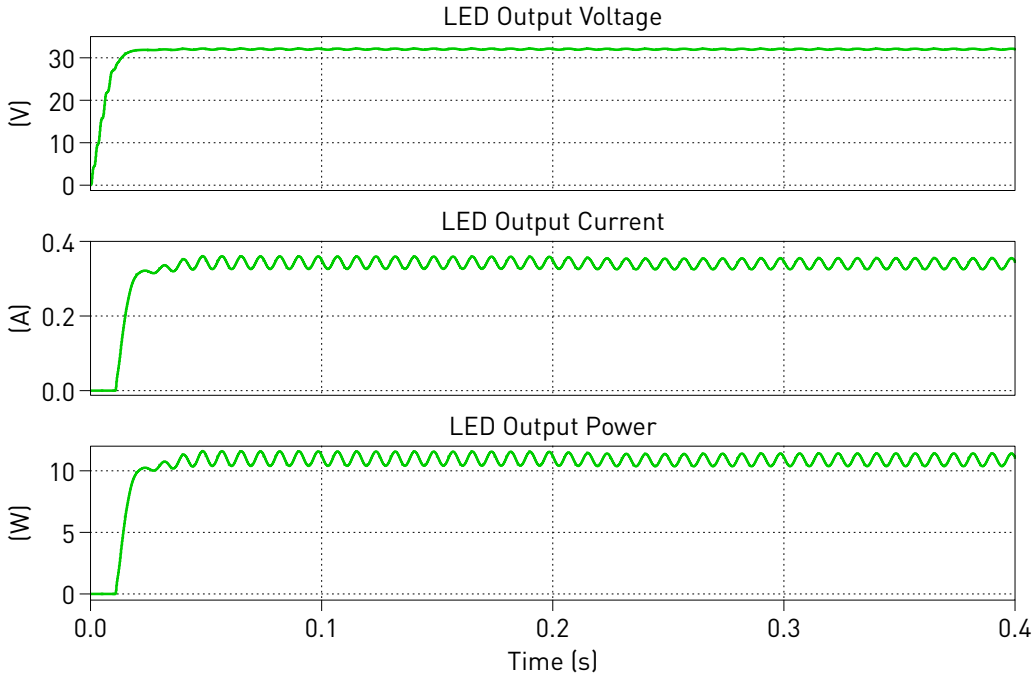

Fig. 3: Simulation result output

Revision History:

PLECS 4.3.1	First release

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PLECS Demo Model