PLECS

DEMO MODEL

LLC Variable Frequency Resonant Converter

Last updated in PLECS 4.9.7

1 Overview

This demonstration shows an isolated DC/DC resonant converter operated under frequency control. The output voltage of the converter is controlled by changing the switching frequency of the semiconductors. Zero-Voltage Switching (ZVS) is used to reduce switching losses, allowing the operation of the converter at higher switching frequencies.

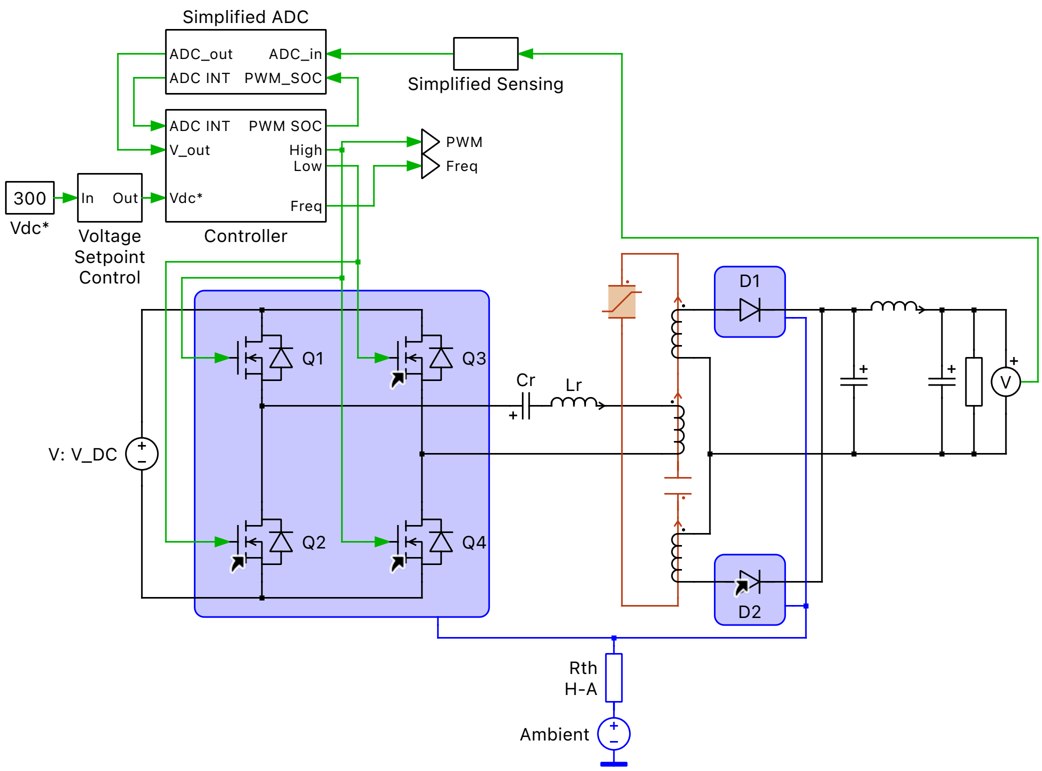

Figure 1: LLC variable frequency resonant converter

Note This model contains model initialization commands that are accessible from:
PLECS Standalone: The menu **Simulation + Simulation Parameters... + Initializations**
PLECS Blockset: Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

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2 Model

2.1 Power Circuit

The LLC converter is a DC/DC converter with a front end H-bridge. The AC side of the H-bridge is connected to the primary side of a high frequency transformer via a series-connected resonant inductor and capacitor. The magnetizing inductance of the transformer, along with the inductor and capacitor, form the LLC resonant tank. The secondary side of the transformer is connected to a full wave diode rectifier to convert the AC transformer output to a high ripple DC voltage that is then filtered to provide a low ripple DC voltage output.

The LLC converter is often operated under zero-voltage switching (ZVS) operation where each FET (e.g., Q1) is turned on when the current is still flowing in its respective anti-parallel diode (e.g., D1). Therefore, only the forward voltage drop of the diode is applied to the FET, which is small compared to the DC input voltage. This results in negligible turn-on loss in the device and contributes to the reduction of overall losses. During ZVS operation, the FETs are turned off in a region where they conduct current. This results in hard-switching of the devices, generating turn-off switching losses, as shown below.

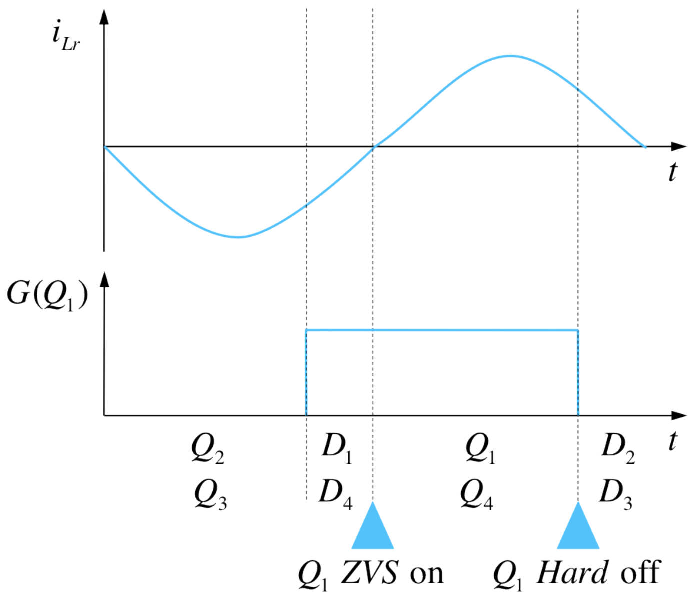

Figure 2: ZVS switching and hard switching

During turn-off and turn-on events, the body capacitor of each FET is charged and discharged, respectively. For circuits where the FETs (not the reverse diodes) experience hard-switching during turn-on, the charge stored in the body capacitor is dissipated through the FET, adding to the switching losses. These losses can be captured in simulation (without adding a capacitor parallel to the FET) by simply including them in the thermal loss look-up tables for a specific part. When measuring the switching energy losses of FETs for certain operation points to generate the loss look-up table, it is important to include the charge stored in the FET body capacitor in the loss measurements. A major advantage of ZVS for FETs, in addition to eliminating turn-on losses, is that the energy stored in the body capacitance is recycled into the circuit [1], assuming there is enough blanking time between turn-off of Q1/Q4 and turn-on of Q2/Q3. Therefore, in soft-switching topologies operated with ZVS, turn-off losses can be overestimated by 10 to $20\,\%$ [2], if the effects of the capacitive elements are not reflected in the loss look-up tables.

2.2 Thermal Model

A thermal description for Wolfspeed's CAS300M12BM2 SiC Half Bridge Module is assigned to all four of the MOSFET switches in the full bridge, and Wolfspeed's C4D40120D SiC Schottky Diode is assigned to the output diodes. If we double-click on any of the MOSFETs we see that a custom masked subsystem is used to implement the various electrical and thermal parameters. To visualize the thermal descriptions of semiconductors that are inside masked subsystems, the easier way is to do so via the **Window + Thermal Library Browser** menu. The diode descriptions can be viewed and edited by double-clicking on the component and selecting **Edit...** from the drop-down menu of the **Thermal description** parameter. The thermal descriptions have been obtained from the Wolfspeed website. For the two different device types, the thermal impedance chain representing the thermal transitions from the junction to the case are entered directly in the thermal descriptions.

Also note that the diode model was customized to permit modeling multiple devices connected in parallel. The number of parallel connections can be configured in the parameter window of the diode. An equal distribution of current and voltage in parallel-connected diodes is assumed. The thermal parameters are automatically scaled to reflect the number of devices and their configuration.

Since the three heat sink components are connected together, all six devices dissipate heat into the same heat sink. A thermal resistance connects the heat sink with the temperature of the ambient air. The thermal descriptions for the MOSFETs and diodes are stored in a private thermal library in the directory `/llc_variable_frequency_resonant_converter_plecs`.

The switching frequency of the model is varying, therefore the average switching and conduction losses are calculated using the "Variable Impulse Avg" and "Variable Avg" subsystems, respectively. These subsystems work similar to the "Periodic Impulse Average" and "Periodic Average" blocks, but can support a variable PWM.

For more information on thermal modeling and the calculation of device losses and efficiency, see the demo model "Buck Converter with Thermal Model" in the PLECS demo models library.

2.3 Controls

The output voltage is measured by a sensing circuit, simplified here as a transfer function (representing a low pass filter). A simplified ADC module is use to convert the measured voltage into its corresponding digital value. The output voltage measurement is compared against a DC voltage set point. The error is fed into a 2-pole, 2-zero implementation of a digital PI controller [3]. An ADC interrupt is used to trigger the interrupt service routine to run the controls (simulated here as a triggered subsystem). The controls generate a counter period set point that is then converted into a frequency set point. The frequency set point is used by the PLECS variable frequency PWM block. The half-bridge FETs are switched with a $50\,\%$ duty cycle.

3 Simulation

A $200\,\mathrm{V}$ input is connected to the DC side of the full bridge. To limit the rate of change in output voltage during reference transitions, a slew rate is applied to the converter. This is reflected in the startup transient, where the output voltage ramps up gradually. A voltage controller is used to control the full bridge switching frequency. The system reaches the desired reference $V_o^* = 300\,\mathrm{V}$ after $17\,\mathrm{ms}$, as shown in Fig. 3. A steady MOSFET junction temperature is achieved after $6\,\mathrm{s}$, as shown in Fig. 4. The applied soft switching strategy ensures safe FET junction temperatures while switching at high frequency.

The LLC converter is simulated twice: once with an output voltage reference of $V_o^* = 300\,\mathrm{V}$ (Nominal operating point) and once with $V_o^* = 250\,\mathrm{V}$.

At the nominal operating point ($V_o^* = 300\,\mathrm{V}$, steady state), the LLC operates with a switching frequency close to the resonant frequency of the resonant tank. The calculated resonant frequency is $f_0 \approx 100\,\mathrm{kHz}$, while the simulated switching frequency is $f_s \approx 103\,\mathrm{kHz}$. Hence, $f_s \approx f_0$ for $V_o \approx 300\,\mathrm{V}$. At this operating point, the output power is $30\,\mathrm{kW}$ and an efficiency of $98.2\,\%$ is achieved.

At the operating point with reduced voltage ($V_o^* = 250\,\mathrm{V}$, steady state), the LLC operates in "Buck Mode", with a switching frequency above the resonant frequency, $f_s \approx 120\,\mathrm{kHz}$. Thus, $f_s > f_0$ for $V_o \approx 250\,\mathrm{V}$. The output power is $20.8\,\mathrm{kW}$, and the efficiency drops to $96.6\,\%$.

Figures 6 and 7 show steady-state simulation results at $V_o^* = 300\,\mathrm{V}$. In Fig. 6, the resonant tank inductor current exhibits a nearly sinusoidal waveform, indicating operation near resonance. From the MOSFET signals in Fig. 7, it is evident that switching losses occur only at turn-off events, with zero turn-on switching losses.

Figures 8 and 9 show steady-state simulation results at $V_o^* = 250\,\mathrm{V}$. Fig. 9 shows that the MOSFET current is turned off at a higher level compared to Fig. 7, resulting in increased turn-off losses and a resonant tank inductor current that deviates more from a sinusoidal shape.

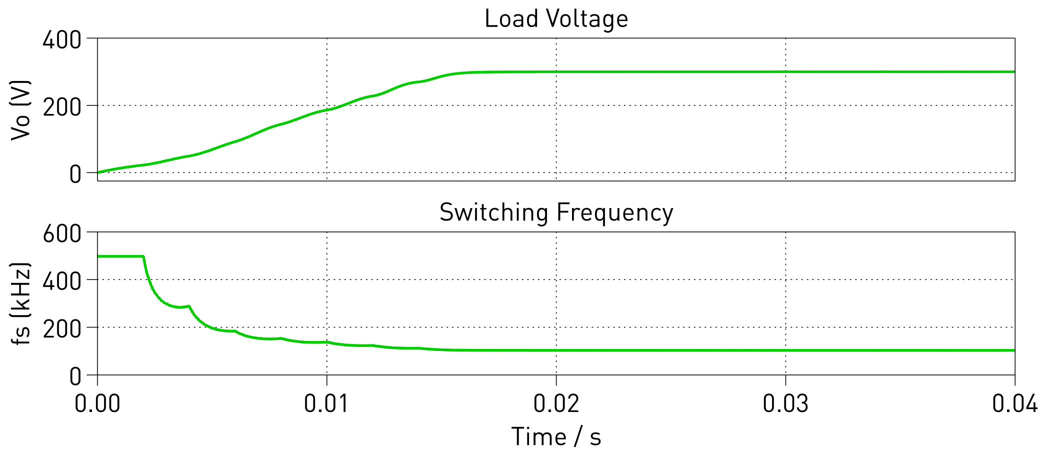

Figure 3: Transient response of the output voltage and switching frequency for 300 V output reference

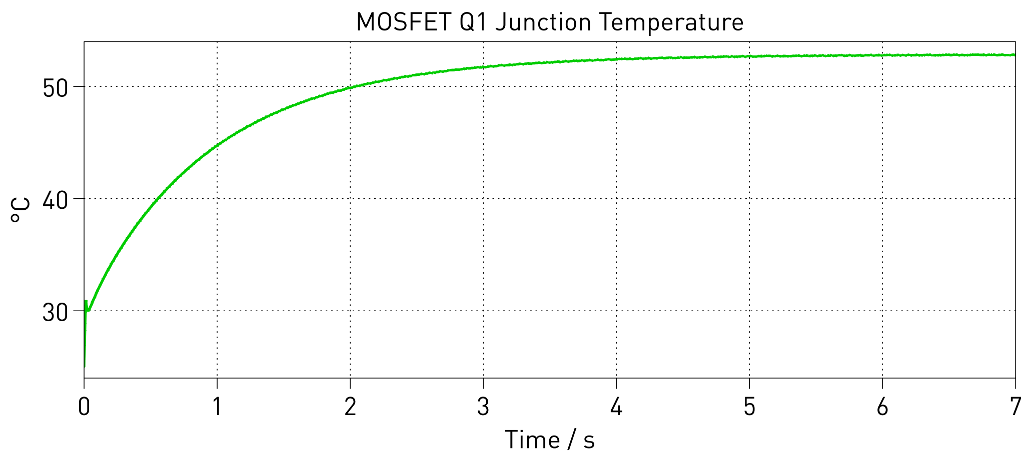

Figure 4: MOSFET junction temperature approaching steady state for 300 V output reference

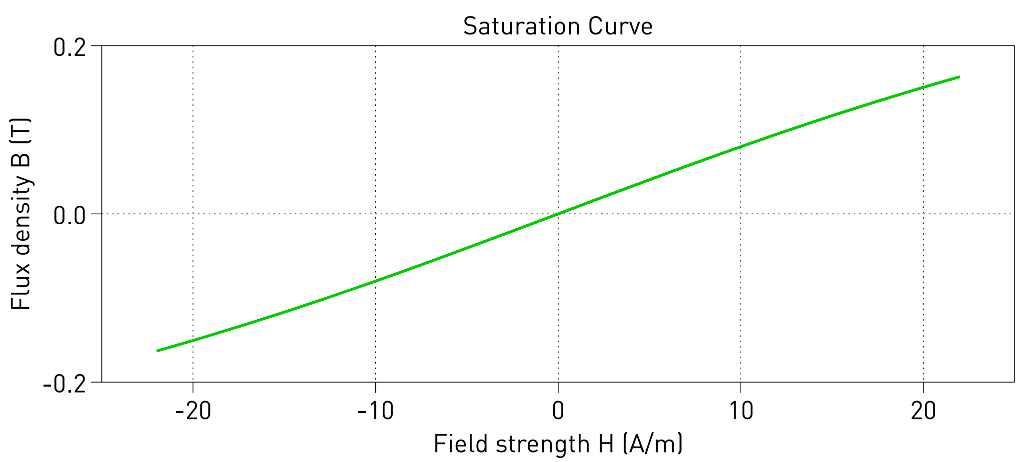

Figure 5: Simulated B-H curve of the transformer core

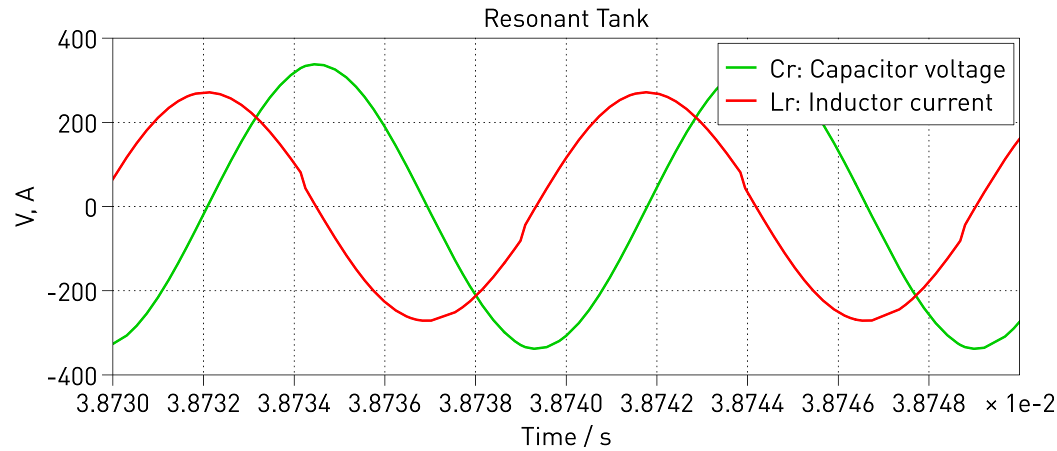

Figure 6: Steady-state resonant tank signals for 300 V output reference

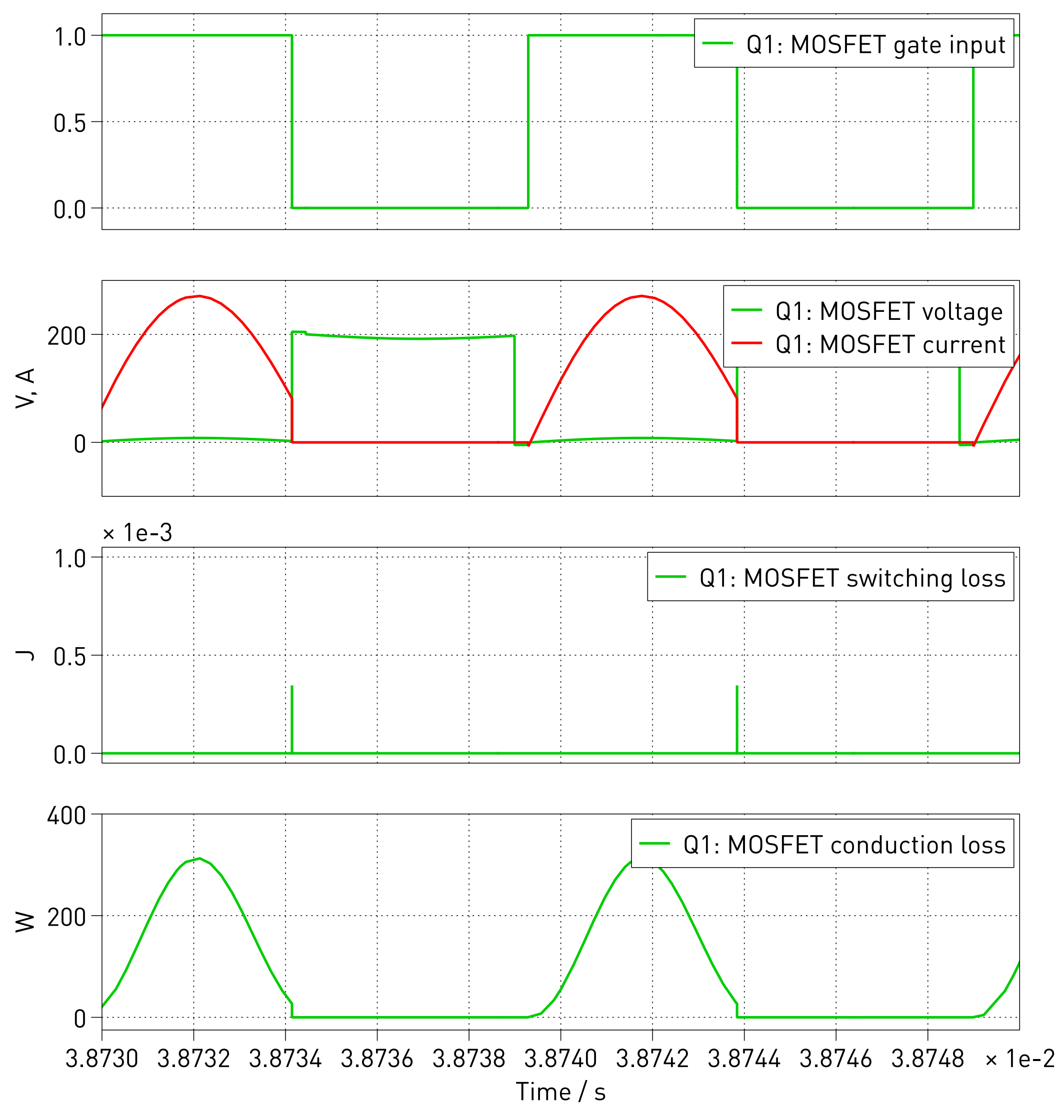

Figure 7: Steady-state MOSFET signals for 300 V output reference

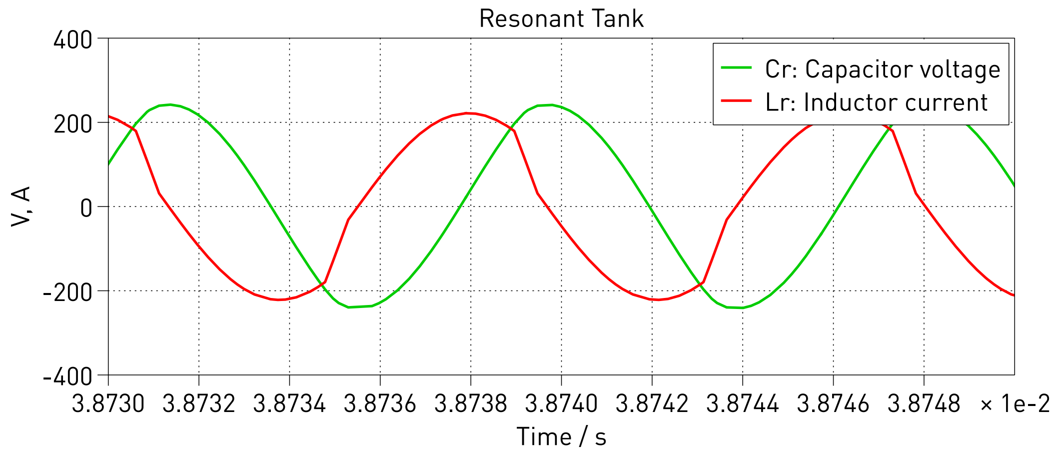

Figure 8: Steady-state resonant tank signals for 250 V output reference

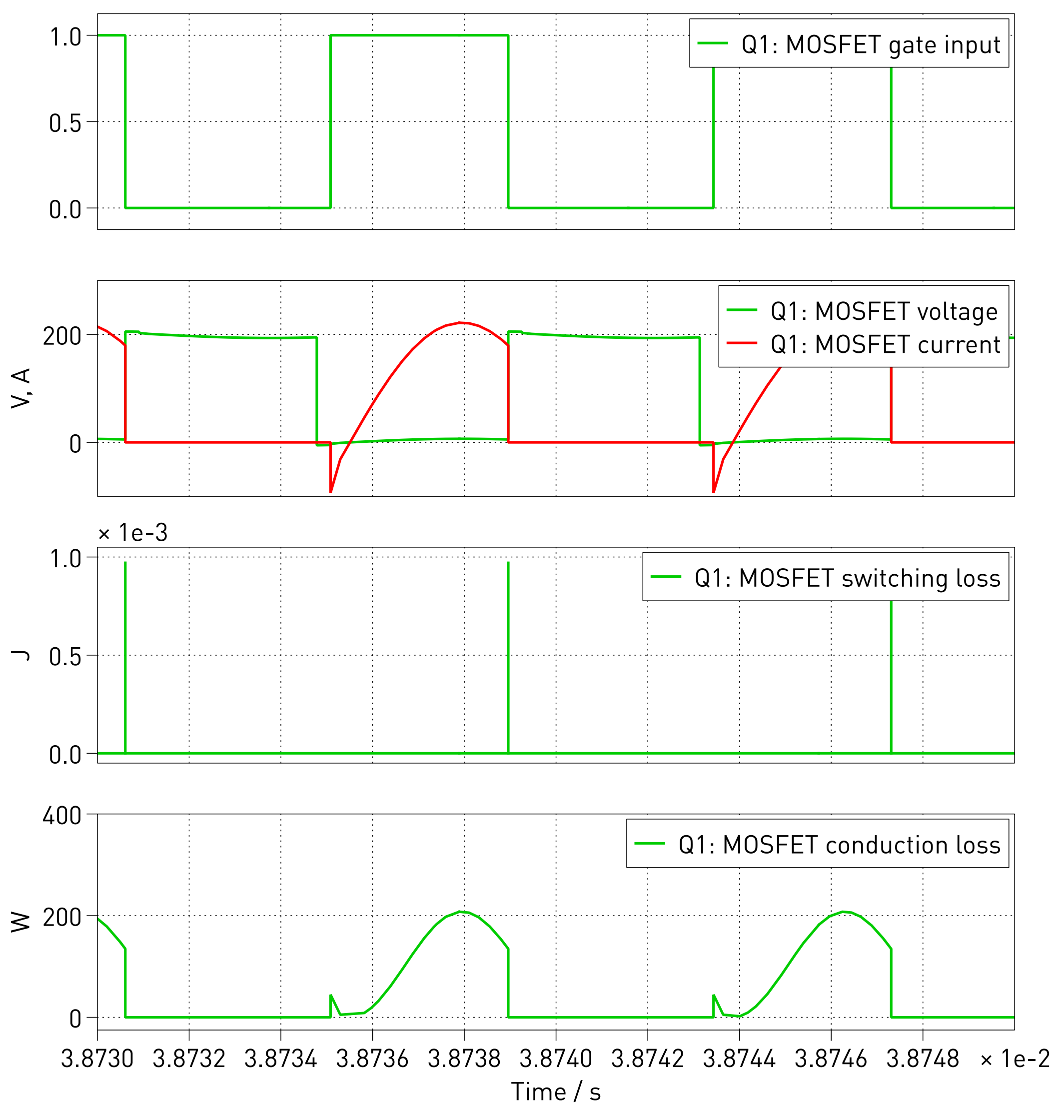

Figure 9: Steady-state MOSFET signals for 250 V output reference

References

[1] R. Erickson and D. Maksimovic "Fundamentals of Power Electronics", 2nd Edition, Springer, 2001, Chapter 19.

[2] "A More Realistic Characterization of Power MOSFET Output Capacitance Coss", International Rectifier Application Note, AN-1001.

[3] Digital Power Control Lab "LLC Resonant Converter", Version 1.1, Texas Instruments, Jan 2009.

Revision History:

PLECS 4.3.1	First release
PLECS 4.7.2	Modified the semiconductor devices; added loss calculation; added variable frequency PWM library block
PLECS 4.9.7	Redesign the converter to improve its thermal behavior

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PLECS Demo Model