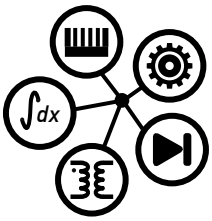

PLECS

DEMO MODEL

Power Supply Compensator Analysis

Last updated in PLECS 4.3.1

1 Overview

This demonstration analyzes the performance of Type 2 and Type 3 analog compensators used in power supply units (PSUs). The analyzed PSU is a buck converter with modeled-in inductor and capacitor non-idealities. The role of the capacitor and its effective series resistance (ESR) on the plant zero and poles is discussed. Furthermore, the compensators' performance is analyzed with respect to the phase margin, system bandwidth, and rate of change in gain at the cross-over frequency. This analysis is based on [1].

Note This model contains model initialization commands that are accessible from:
PLECS Standalone: The menu **Simulation + Simulation Parameters... + Initializations**
PLECS Blockset: Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

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2 Model

2.1 Power circuit

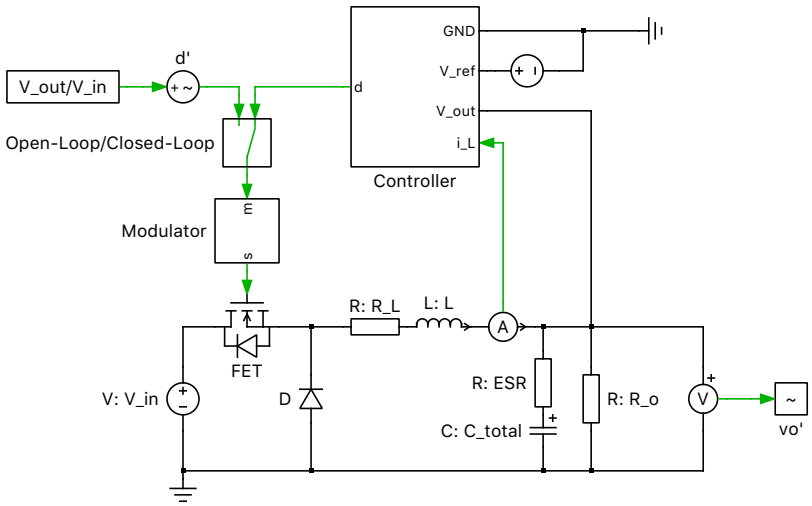

Figure 1: Type 2 and type 3 compensator analysis for power supplies (PLECS Standalone)

The analyzed PSU is a simple buck converter where the capacitance and ESR effects are being investigated. The plant transfer function can be simplified to the following:

$$G_{\text{plant}}(s) = \frac{R_{\text{o}}(C_{\text{total}} \cdot ESR \cdot s + 1)}{L \cdot C_{\text{total}} \cdot s^2(R_{\text{o}} + ESR) + s(L + R_{\text{o}} \cdot C_{\text{total}} \cdot ESR) + R_{\text{o}}}$$

where the Laplace operator, "s", and thus the plant transfer function, varies as a function of the frequency. In $G_{\text{plant}}(s)$, the effects of the inductor resistance are assumed to be minimal on system performance and, thus, ignored. For the buck converter, the system double poles and zero due to the LC-filter and ESR, respectively, are given by:

$$f_{\text{LC}} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{\text{total}}}}$$

$$f_{\text{ESR}} = \frac{1}{2 \cdot \pi \cdot C_{\text{total}} \cdot ESR}$$

The voltage controllers are designed by placing the system poles and zeros such that the loop gain of the closed-loop system has desired characteristics.

2.2 Control

The model can be run either as an open-loop or closed-loop controlled system. Double-clicking on the Manual Switch ("Open-Loop/Closed-Loop") toggles the model configuration.

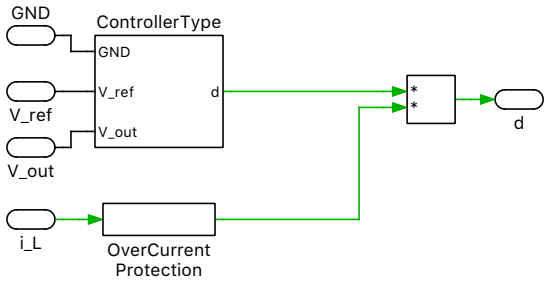

Figure 2: Closed-loop controller schematic

The closed-loop control system consists of a voltage-mode regulator and over-current protection. The voltage-mode regulator can be configured to operate either with a Type 2 or Type 3 compensator.

The loop gain should have the following characteristics to ensure high dynamics and stability of the closed-loop system:

- A cross-over frequency between $\frac{1}{10}$ and $\frac{1}{5}$ of the switching frequency.
- A $-20\,\mathrm{dB}$ per decade slope of the gain near the system cross-over frequency.
- A phase margin greater than $45°$.

Type 2 Compensator

Type 2 compensators are used in systems where the desired cross-over frequency (f_x) is greater than both f_LC and f_ESR. That is:

$$f_\mathrm{LC} < f_\mathrm{ESR} < f_\mathrm{x} < f_\mathrm{sw}/2$$

where $f_\mathrm{sw}/2$ is half the switching frequency. We will refer to this as System 1.

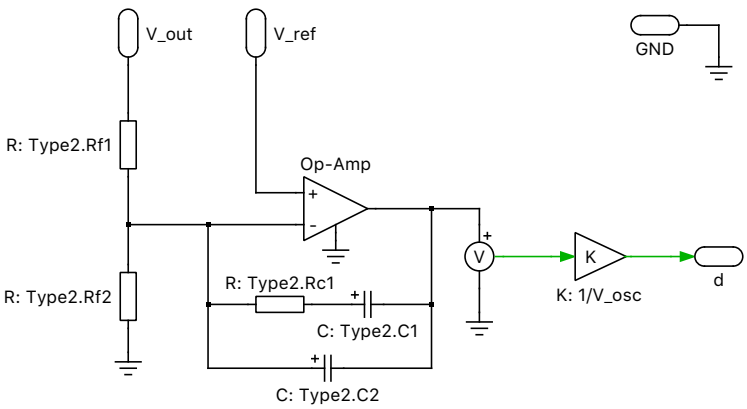

Figure 3: Type 2 compensator circuit

The Type 2 compensator in the model shown above is implemented using an ideal op-amp with finite gain. The op-amp gain is set to 10^6. The positive input terminal is connected to the reference voltage. The output voltage of the buck converter is scaled using a resistive divider and connected to the negative

input terminal of the op-amp. Furthermore, the negative input is connected to the op-amp output via an RC network. The simplified transfer function of the Type 2 compensator (Eq. 9 in [1]) is given by:

$$H_{\mathrm{Type2}}(s) \approx \frac{1 + C_1 \cdot R_{\mathrm{C1}} \cdot s}{C_1 \cdot R_{11} \cdot s(1 + C_2 \cdot R_{\mathrm{C1}} \cdot s)}$$

The zero and poles of the compensator are given by:

$$f_{\mathrm{z1}} = \frac{1}{2 \cdot \pi \cdot C_1 \cdot R_{\mathrm{C1}}}$$

$$f_{\mathrm{p1}} = 0$$

$$f_{\mathrm{p2}} = \frac{1}{2 \cdot \pi \cdot C_2 \cdot R_{\mathrm{C1}}}$$

To obtain the desired system performance, the resistors and capacitors can be selected to ensure that:

$$f_{\mathrm{z1}} \approx 0.75 \cdot f_{\mathrm{LC}}$$

$$f_{\mathrm{p2}} \approx f_{\mathrm{sw}}/2$$

Placing the zero and pole at these locations, along with the pole at the origin (f_{p1}), causes the loop gain of the closed-loop system to exhibit the desired characteristics.

Type 3 Compensator

In systems where f_{x} is less than f_{ESR}, the Type 2 compensator may not be able to provide the desired closed-loop system response and stability. A Type 3 compensator can then be used.

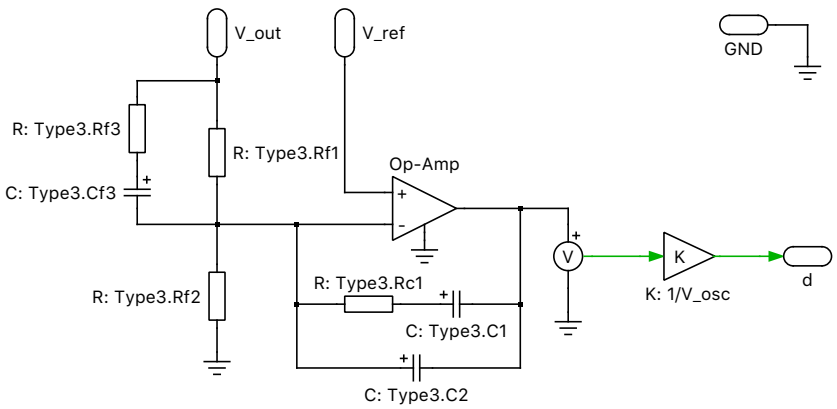

Figure 4: Type 3 compensator circuit

As with the Type 2 compensator, the Type 3 compensator is implemented with an ideal, finite-gain op-amp. The Type 3 compensator configuration is shown above. For systems where:

$$f_{\mathrm{LC}} < f_{\mathrm{x}} < f_{\mathrm{ESR}} < f_{\mathrm{sw}}/2$$

the additional pole and zero of the Type 3 compensator allow for the design of a fast and stable closed-loop control of this system. We will refer to this as System 2. The simplified transfer function of the Type 3 compensator (Eq. 22 in [1]) is given by:

$$H_{\mathrm{Type3}}(s) \approx \frac{(1 + C_1 \cdot R_{\mathrm{C1}} \cdot s) \cdot (1 + C_{\mathrm{f3}} \cdot (R_{\mathrm{f1}} + R_{\mathrm{f3}}))}{C_1 \cdot R_{\mathrm{f1}} \cdot s(1 + C_2 \cdot R_{\mathrm{C1}} \cdot s) \cdot (1 + C_{\mathrm{f3}} \cdot R_{\mathrm{f3}} \cdot s)}$$

The zero and poles of the compensator are given by:

$$f_{z1} = \frac{1}{2 \cdot \pi \cdot C_1 \cdot R_{C1}}$$

$$f_{z2} = \frac{1}{2 \cdot \pi \cdot C_{f3} \cdot (R_{f1} + R_{f3})}$$

$$f_{p1} = 0$$

$$f_{p2} = \frac{1}{2 \cdot \pi \cdot C_{f3} \cdot R_{f3}}$$

$$f_{p3} = \frac{1}{2 \cdot \pi \cdot C_2 \cdot R_{C1}}$$

To obtain the desired system performance, the resistors and capacitors can be selected to ensure that:

$$f_{z1} \approx 0.75 \cdot f_{LC}$$

$$f_{z2} \approx f_{LC}$$

$$f_{p2} \approx f_{ESR}$$

$$f_{p3} \approx f_{sw}/2$$

Placing the zeros and poles at these locations, along with the pole at the origin (f_{p1}) causes the loop gain of the closed-loop system to demonstrate the desired characteristics.

Overcurrent protection

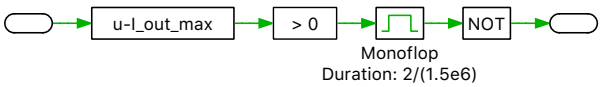

Figure 5: Overcurrent protection circuit

An IR3840 synchronous buck regulator based over current protection is modeled in this circuit. This is used to limit the current that is drawn from the input voltage source. As the current through the inductor reaches the maximum allowable current in the system, the switching modulation index is set to 0. After a few clock cycles the over current protection system is reset.

3 Simulation

The model has been configured to emulate the two different systems described above. The variable `CapSelector` is used to toggle between the two systems. In PLECS Standalone and PLECS Blockset this variable can be accessed and changed the following way:

- *Standalone:* Open the **Initialization** tab under **Simulation + Simulation parameters...** and set a value in line #13
- *Blockset:* Open the Simulink menu **File + Model Properties** Then in the **Callbacks** tab choose the **InitFcn*** and set a value in line #13

Open-loop control analysis

In the compensator design process, the open-loop plant transfer function is used to verify the analytical model of the plant. With the model as is, execute the following steps for either PLECS Standalone or PLECS Blockset:

- *Standalone:* Select **Analysis tools...** from the **Simulation** menu. Run either the Multitone or Impulse Response Analysis for the "Control to Output TF" analysis. This provides the transfer function for the open-loop system.
- *Blockset:* Double-click on the Impulse Response Analysis or Loop Gain (Multitone) blocks on the Simulink level to open the respective dialogs and click on the **Start analysis** button. The progress of an analysis can be configured for display in the MATLAB Command Window. When the analysis has finished a new Bode plot will be displayed showing the corresponding transfer function.

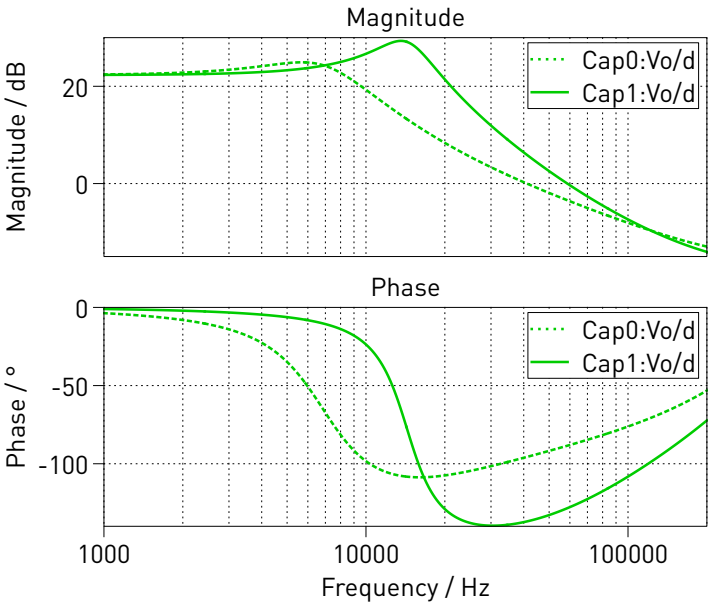

Figure 6: Plant transfer function with different output capacitors (Cap0: $940\,\mu$F, ESR=$10\,\mathrm{m}\Omega$ and Cap1: $220\,\mu$F, ESR=$8\,\mathrm{m}\Omega$)

Observe the Bode plot generated by the analysis (dashed line). The cross-over frequency is about $40\,\mathrm{kHz}$, and the slope is close to $-20\,\mathrm{dB}$ per decade. The phase margin is about $95°$. While the slope and phase margin are desirable, the cross-over frequency remains lower than $60\,\mathrm{kHz}$, which is $1/10$ of the switching frequency. Thus, the system has a slower dynamic response than desired.

Change the variable `CapSelector` to 1 as described above. Re-run the previous analysis.

Observe the new Bode plot generated by the analysis (solid line). The cross-over frequency is about $60\,\mathrm{kHz}$ and the phase margin is about $50°$. While the cross-over frequency and phase margin are desirable, the slope of the gain curve around the cross-over frequency is close to $-40\,\mathrm{dB}$ per decade. This may result in an unstable system.

Closed-loop control analysis: system 1

Reset the `CapSelector` to 0 as described above. Double-click on the manual switch "Open-Loop/Closed-Loop" to configure the model for closed-loop control operation. Run the Loop Gain Analysis (in PLECS Standalone "System 1 - Loop Gain Analysis") to obtain the loop gain of the closed-loop system.

Analyze the Bode plot generated by the analysis. The cross-over frequency is about $65\,\mathrm{kHz}$, the slope of the gain is close to $-20\,\mathrm{dB}$ per decade, and the phase margin is about $65°$. Thus, the system has the desired stability and dynamics (dashed line in Fig. 7).

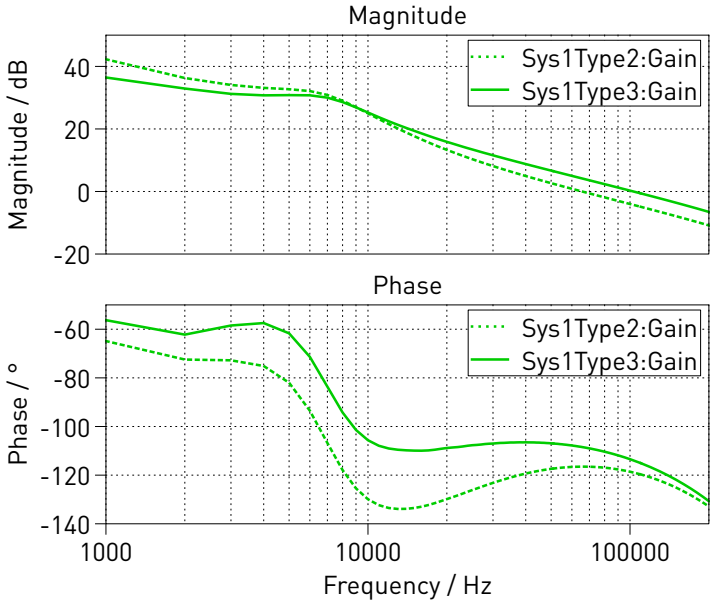

Figure 7: Loop gain of the closed-loop System 1 with Type 2 and Type 3 controller

Next, in the controller subsystem, change the controller type from Type 2 to Type 3. Re-run the same analysis. Observe the Bode plot generated by the analysis. The cross-over frequency is about $100\,\mathrm{kHz}$, the slope of the gain is close to $-20\,\mathrm{dB}$ per decade, and the phase margin is about $65°$. Thus, this system also has the desired stability and dynamics (solid line in Fig. 7).

Closed-loop control analysis: system 2

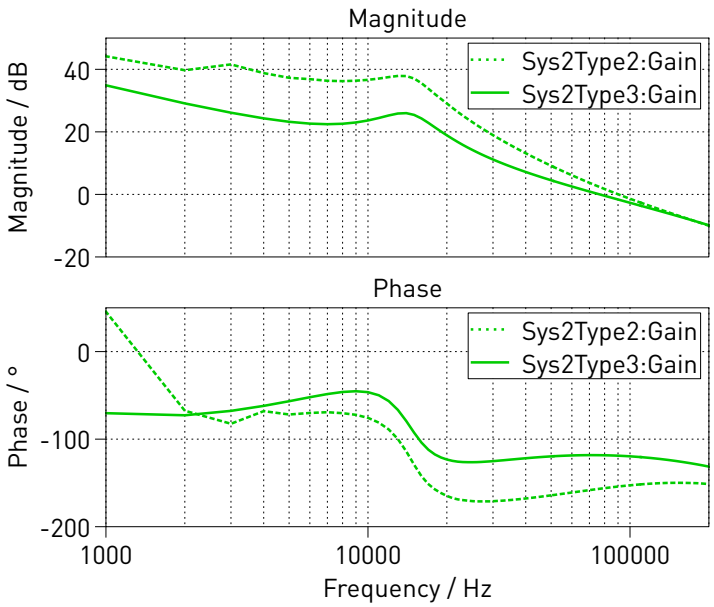

Figure 8: Loop gain of the closed-loop System 2 with Type 2 and Type 3 controller

Next, change the `CapSelector` to 1 as described above. Run the Loop Gain Analysis (in PLECS Standalone "System 2 - Loop Gain Analysis") to obtain the loop gain of the closed-loop system. The cross-over frequency is about $75\,\mathrm{kHz}$, the slope of the gain is close to $-20\,\mathrm{dB}$ per decade, and the phase margin is about $61°$. Thus, this system also has the desired stability and dynamics.

Next, in the controller subsystem, change the controller type from Type 3 to Type 2. Re-run the same analysis. The cross-over frequency is about $92\,\mathrm{kHz}$. However, the slope of the gain is close to $-40\,\mathrm{dB}$ per decade, and the phase margin is about $25°$. Thus, the Type 2 compensator is unable to meet the system stability requirements for System 2.

References

[1] A. M. Rahimi, P. Parto, P. Asadi, "Compensator Design Procedure for Buck Converter with Voltage-Mode Error-Amplifier", *International Rectifier Application Note AN-1162*.

Revision History:

PLECS 4.3.1	First release

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PLECS Demo Model