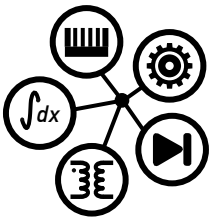

PLECS

DEMO MODEL

Vienna Rectifier with Hysteresis Controller

Last updated in PLECS 4.3.1

1 Overview

This demonstration shows a Vienna Rectifier with an output voltage of $700\,\mathrm{V}$ and an output power of $12.25\,\mathrm{kW}$. The simulation combines the electrical power circuit and the cascaded controls.

2 Model

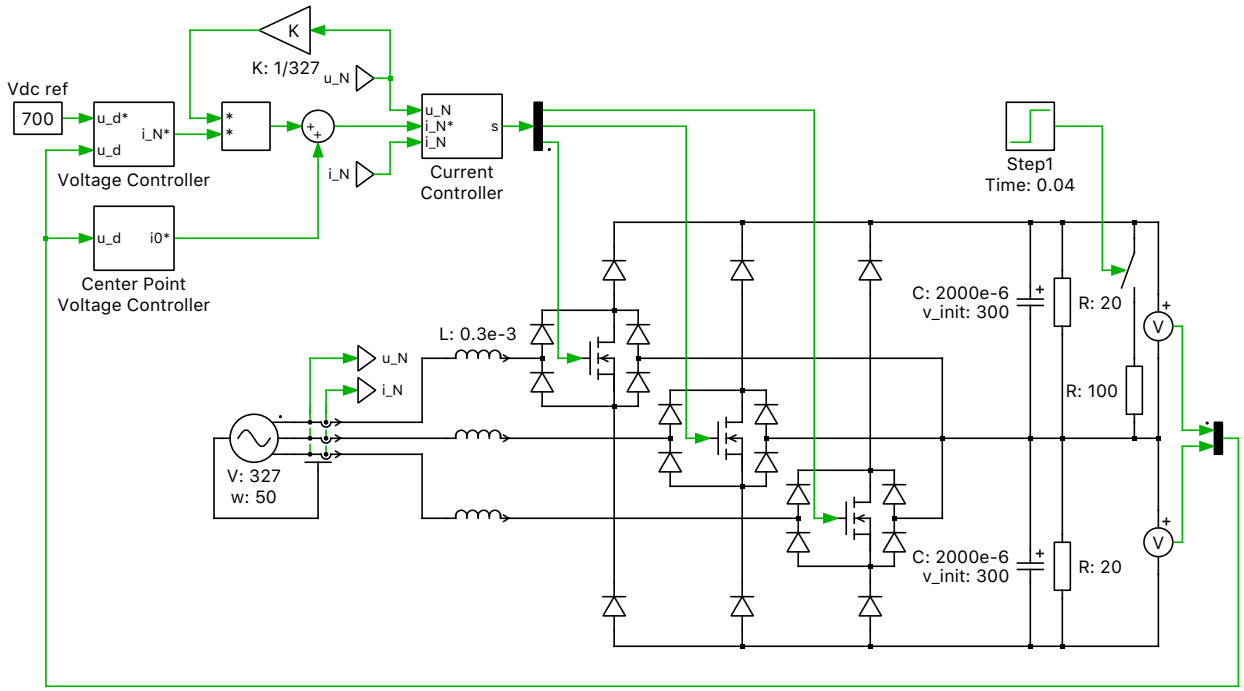

Figure 1: Vienna rectifier

The Vienna Rectifier is a unidirectional, three-phase, three-switch, three-level PWM AC-DC converter.

2.1 Control

The controls are modeled as cascaded subsystems and consist of a current loop, a DC center point voltage loop and a DC voltage loop.

The outermost DC voltage loop regulates the sum of the two capacitor voltages using a PI controller. The controller output is the reference for the mains current amplitude I_N^*. This amplitude is multiplied with a three-phase sinusoidal signal which is synchronized with the mains voltages in order to obtain the three-phase mains current reference I_N^*. For simplicity, this sinusoidal signal is generated directly from the measured mains voltages.

The mains current reference signal is offset by a DC current reference I_0^*. This DC reference is the output of a PI controller regulating the difference of the two capacitor voltages.

Finally, the mains current reference signal is used by the hysteresis current controller to generate the gate signals for the semiconductor switches. Due to the operating principle of the Vienna Rectifier, the gate signal of an individual phase needs to be inverted during the negative half-wave of the corresponding mains phase voltage.

3 Simulation

The simulation shows the controller response to a sudden asymmetrical loading of the output voltage. The Scope shows the sinusoidal mains voltage, the hysteresis controlled mains current and DC voltages of the two output capacitors.

At simulation start, the capacitors are charged from their initial $300\,\mathrm{V}$ to their nominal level at $350\,\mathrm{V}$. At t = $0.4\,\mathrm{s}$, the load becomes unbalanced. Without the center point voltage controller, the capacitor voltages would also quickly become unbalanced. With the controller in operation there is only a small deviation, and the capacitors are balanced again after about $0.1\,\mathrm{s}$.

References

[1] Kolar J.W., Zach F.C., “A Novel Three-Phase Utility Interface Minimizing Line Current Harmonics of High-Power Telecommunications Rectifier Modules”. Record of the 16th IEEE International Telecommunications Energy Conference, Vancouver, Canada, Oct. 30 - Nov. 3, pp. 367-374 (1994).

[2] Kolar J.W., Drofenik. U., Zach F.C. “Space Vector Based Analysis of the Variation and Control of the Neutral Point Potential of Hysteresis Current Controlled Three-Phase/Switch/Level PWM Rectifier Systems”. Proceedings of the International Conference on Power Electronics and Drive Systems, Singapore, Feb.21-24, Vol.1, pp. 22-33 (1995).

Revision History:

PLECS 4.3.1	First release

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PLECS Demo Model