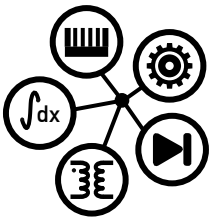

PLECS

DEMO MODEL

PLECS Spice - Buck Converter with Controller

This model demonstrates the simulation of parasitic effects in power electronics using PLECS Spice. A buck converter is implemented using both standard PLECS components and PLECS Spice netlists, with seamless switching between modeling approaches through subsystem configuration.

Last updated in PLECS 5.0.1

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1 Model Overview

This demo showcases how PLECS Spice enables seamless transition from ideal switch models to detailed SPICE-based semiconductor models in a Buck converter application. The aim of the model is to showcase how a PLECS model can be used to tune the control loop of a power converter using ideal switch models, and then easily switch to a more detailed SPICE-based semiconductor model for more accurate simulation of switching behavior. The overall schematic is depicted in Fig. 1.

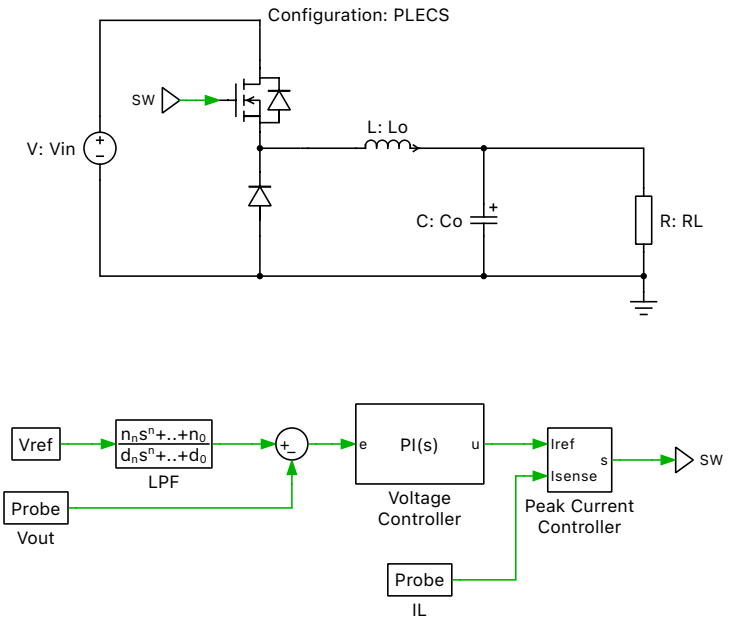

Fig. 1: Model schematic.

Note

This model contains model initialization commands that are accessible from:
PLECS Standalone: the menu **Simulation > Simulation Parameters... > Initializations**

1.1 Controller

The controller chosen for this converter is a cascaded closed-loop controller, comprising an outer voltage controller and an inner current control loop, as shown in the bottom part of Fig. 1. The voltage controller is implemented with a PI regulator built with the Continuous PID Controller[1] from the PLECS component library. Additionally, a filter on the voltage reference has been included using the Transfer Function[2] block. The inner current control is implemented using the Peak Current Controller[3] block from the PLECS component library. Overall the control structure is similar to the one presented in the ”Buck Converter with Peak Current Control”.

1.2 Power Stage

The power stage of the Buck converter features a configurable subsystem containing both power semiconductors. This allows to easily switch form the ideal switch modelling of PLECS to a more detailed SPICE-based semiconductor model.

[1] https://docs.plexim.com/plecs/latest/components-by-category/continuouspidcontroller/#component-continuouspidcontroller
[2] https://docs.plexim.com/plecs/latest/components-by-category/transferfcn/#component-transferfcn
[3] https://docs.plexim.com/plecs/latest/components-by-category/peakcurrentcontroller/#component-peakcurrentcontroller

PLECS Configuration

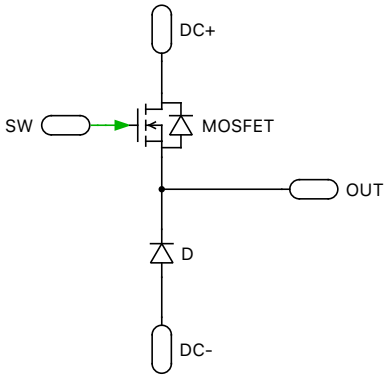

Fig. 2: PLECS configuration.

In Fig. 2, the PLECS configuration of the power stage is depicted. Here, both the MOSFET with Diode[4] and Diode[5] are modelled using ideal switches available in the PLECS library. It is worth highlighting that the switching signal, indicated by the green color, drives the MOSFET gate directly. The MOSFET turns on instantaneously whenever a non-zero signal is applied to its gate. Conversely, it turns off instantaneously when the gate signal is removed. The diode is also modelled as an ideal switch that turns on and off instantaneously based on the voltage across its terminals. This approach allows for fast simulation times, making it suitable for control design and system-level studies.

SPICE Configuration

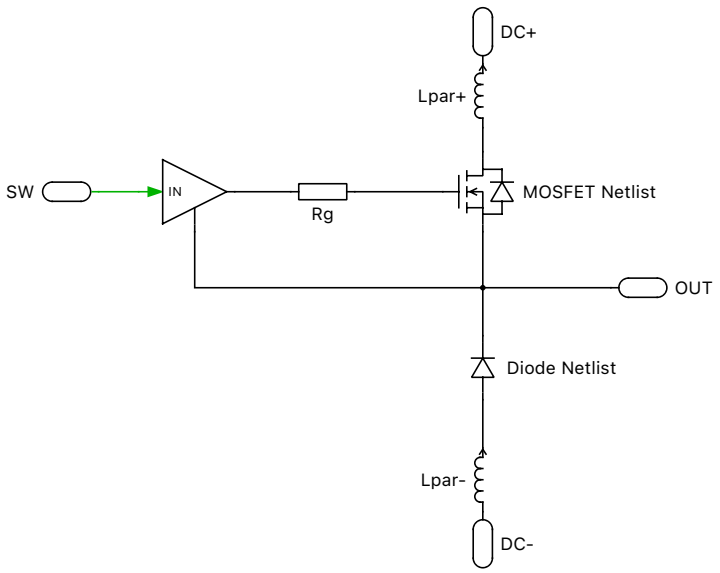

Fig. 3: SPICE configuration.

The SPICE configuration of the power stage is illustrated in Fig. 3. Here, the ideal switch models of the MOSFET and diode are replaced with detailed SPICE netlists using the Netlist[6] block provided by the PLECS component library. These netlists capture the technology-dependent non-ideal switching behavior of the semiconductors, including turn-on and turn-off transients and the impact of the parasitic ca-

[4] https://docs.plexim.com/plecs/latest/components-by-category/mosfetwithdiode/#component-mosfetwithdiode
[5] https://docs.plexim.com/plecs/latest/components-by-category/diode/#component-diode
[6] https://docs.plexim.com/plecs/latest/components-by-category/netlist/#component-netlist

pacitances and inductances. Additionally, parasitic inductances are included to model the printed circuit board physical layout effects. This would not be feasible using standard PLECS simulations.

Since netlists live only in the electrical domain, the control signal (shown in green) needs to be converted to a voltage signal that drives the MOSFET gate. For the sake of this demo model, the gate driver circuit, reported in Fig. 4, is minimal. It consists of a Rate Limiter[7] to limit the maximum derivative of the control gate voltage, a Gain[8] block to adapt to the desired voltage level and a Voltage Source (Controlled)[9] to finally convert the control signal into a voltage. However, in practical applications it is also possible to use a netlist to model the gate driver in addition to the power semiconductors.

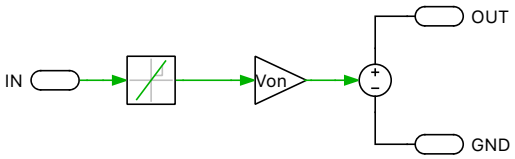

Fig. 4: Gate driver circuit.

By modeling the power semiconductors and the gate driver, the SPICE configuration offers a more accurate representation of the circuit level behavior of the converter, which is useful for detailed design and analysis of the power stage. This comes at the cost of increased simulation time compared to the PLECS configuration. For this example, SPICE models provided by Microchip are used, see [1].

2 Simulation

We recommend that this model is explored by following the steps below.

Begin with the “PLECS” configuration of the power stage (double-click on “Configurable Power Stage” block and select from drop-down list), simulate the model, and observe the waveforms (hold the traces in the scopes for better comparison later). Next, switch to the “SPICE” configuration of the power stage, simulate the model again, and compare the waveforms to those obtained with the “PLECS” configuration. In the following, the results obtained with PLECS are reported with a solid green trace, whereas the SPICE results are shown with a solid red trace.

Simulating the buck converter in both PLECS and SPICE configurations shows only a slight difference in the output voltage regulation, as depicted in Fig. 5. This stems form the additional steady-state series resistances and inductances introduced in the SPICE configuration.

However, looking at MOSFET waveforms reveals more pronounced differences between the two configurations. The drain-source voltage, drain-source current, and gate-source voltage at the MOSFET turn on are reported in Fig. 6 on p. 6. It is immediately possible to notice the delay in MOSFET conduction due to the finite rise time of the gate voltage and the current build up due to the inductive load. Additionally, it is also possible to analyze the gate driver circuit behaviour, including, for example, the gate-source voltage drop due to the Miller effect.

Eventually, in Fig. 7 on p. 7, the diode voltage and current are reported at diode turn off, which is the same time instant as the MOSFET turn on. The SPICE configuration allows to analyze the reverse recovery behavior of the diode, which is tightly related to the MOSFET current overshoot at turn on. This phenomenon is not captured when using ideal diode models in PLECS configuration.

3 Conclusion

By selecting the appropriate configuration of the power stage, it is possible to easily and seamlessly switch between the PLECS and SPICE simulations. This allows to take advantage of the fast simulation

[7] https://docs.plexim.com/plecs/latest/components-by-category/ratelimiter/#component-ratelimiter
[8] https://docs.plexim.com/plecs/latest/components-by-category/gain/#component-gain
[9] https://docs.plexim.com/plecs/latest/components-by-category/controlledvoltagesource/#component-controlledvoltagesource

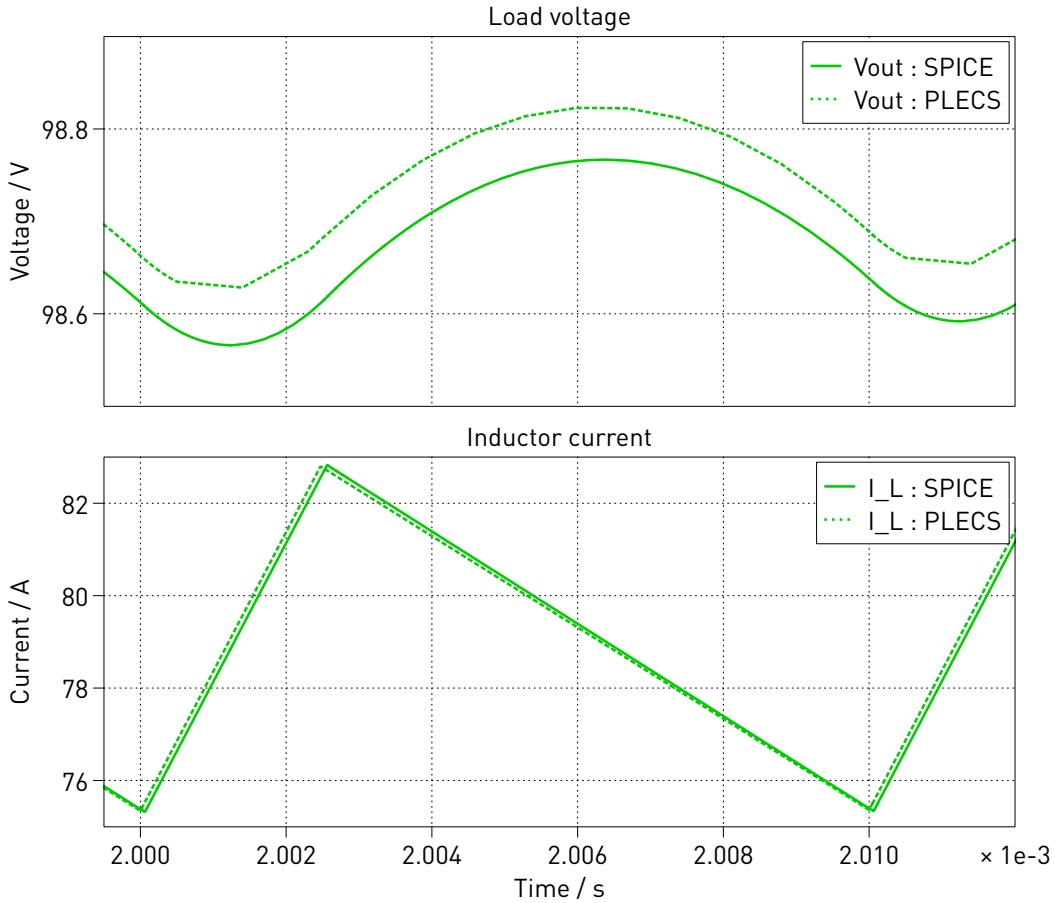

Fig. 5: Load behavior.

times of PLECS ideal switch models for control design and system-level studies, and then switch to detailed SPICE-based semiconductor models for accurate analysis of switching behavior and circuit-level effects.

4 Bibliography

[1] Microchip Silicon Carbide Products SPICE and PLECS Files. Click to access online: Microchip SiC SPICE models[10].

[10] https://www.microchip.com/en-us/software-library/sic-products-spice-files

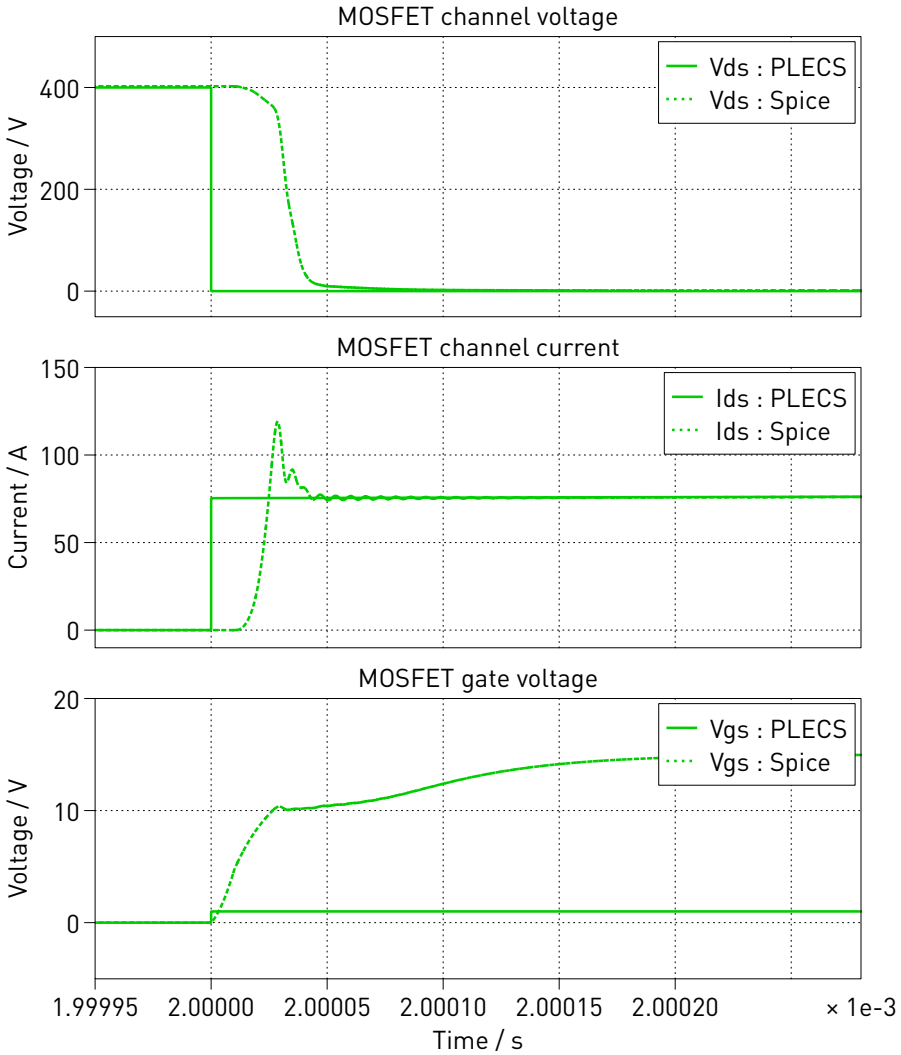

Fig. 6: MOSFET turn on behavior.

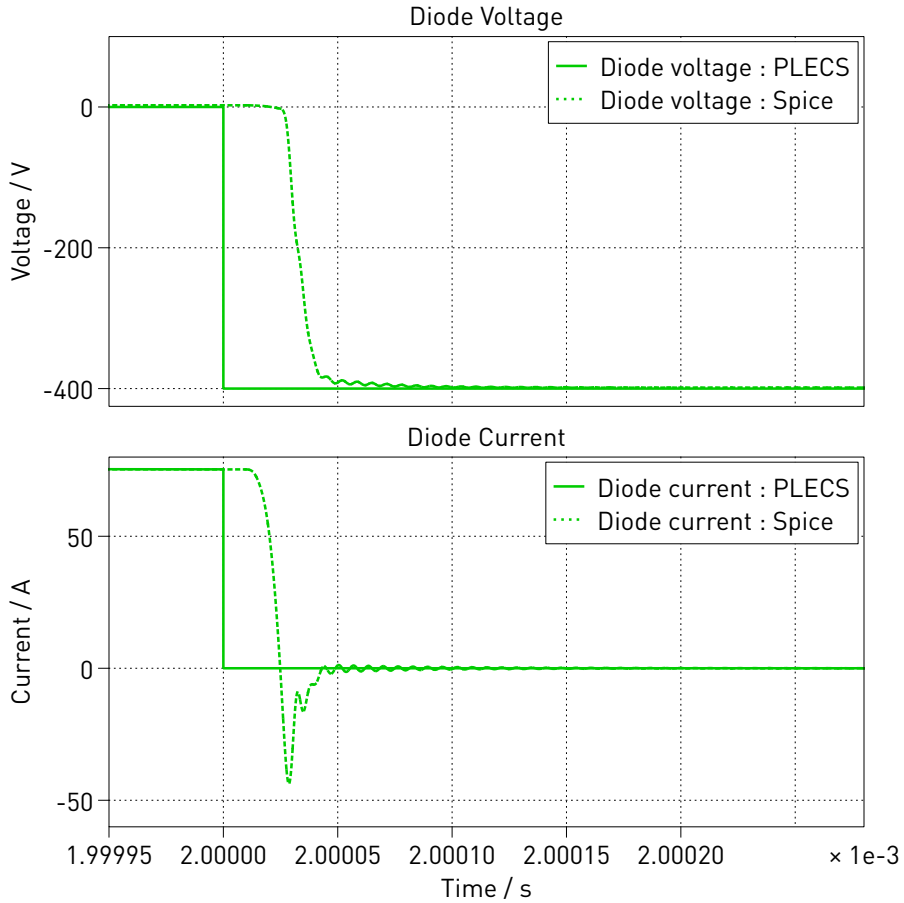

Fig. 7: Diode turn off behavior.

Revision History:

PLECS 5.0.1	First release

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PLECS Demo Model

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