



PLECS

DEMO MODEL

Three-Phase Voltage Source Inverter

Impact of Basic VSI Modulation Schemes on Harmonics

Last updated in PLECS 4.7.1

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1 Overview

This model shows a three-phase voltage source inverter (VSI). The VSI is an inverter circuit which creates AC current and voltage from a DC voltage source. Three different Pulse-Width Modulation (PWM) schemes are presented for controlling the VSI output. The system is designed to achieve a power rating of 10 kW.

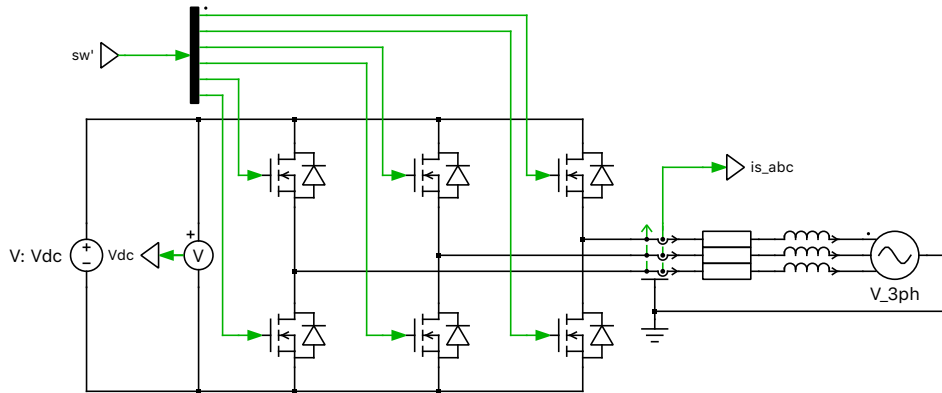


Fig. 1: Three-phase voltage source inverter (VSI)

Note

This model contains model initialization commands that are accessible from:

PLECS Standalone: the menu **Simulation > Simulation Parameters... > Initializations**

PLECS Blockset: right click in the **Simulink model window > Model Properties > Callbacks > InitFcn***

2 Model

2.1 Plant

A 700 V DC voltage source supplies power to the inverter. This DC source could represent any number of systems, such as a battery system, solar array, or rectifier circuit. The inverter connects to a low-voltage (230 V_{rms}) 50 Hz grid system. The low-voltage grid is represented as a stiff AC voltage source.

For grid-tied inverters it is common practice to choose the grid-connecting inductive reactance to be 5 to 10 % of the base impedance rating. For this system, the grid-connecting reactance is 10 % of the base impedance. A small parasitic resistance is also included to model losses in the inductor.

The inductor currents are initialized based on the desired power rating of 10 kW at unity power factor. If the inductor currents were not initialized there would be a transient during start-up until the steady-state operating conditions are reached.

2.2 Controller

A Configurable Subsystem named “Controller” contains three common PWM methods for a VSI: Sine PWM, Space Vector (SV) PWM, and Hysteresis PWM. The Configurable Subsystem includes a dynamic mask where different control parameters may be entered according to the selected modulator type. Choosing different modulator types presents different control parameters.

Typically, the VSI output terminal voltage or reference current would be dynamically calculated using closed-loop control methods but in this model fixed values are used. In each modulator implementation, reference signals are provided that determine the VSI output.

Sine and SV PWM configurations

For the Sine PWM and SV PWM implementations the reference signal is the desired average voltage at the VSI output terminals. The phase shift between the VSI output terminal voltage and the grid voltage determines the VSI output current. The voltage magnitude and angle of the VSI (V_{inv}) required to achieve rated current output (I_{rated}) is applied as a fixed modulation index and phase shift.

The VSI terminal output voltage is determined by representing the balanced three-phase system as single-phase RMS equivalent model. In this case, the grid voltage is considered to be $V_{grid} = 230 V_{rms} \angle 0^\circ$ and the impedance of the series-connected inductor and resistor is $Z = R + 2\pi fL$, where f corresponds to the nominal grid frequency of 50 Hz. The average voltage output required at the VSI terminals to produce such a current is $V_{inv} = V_{grid} + Z \cdot I_{rated}$, where V_{inv} is a complex RMS value.

Note that the Space Vector PWM switching sequence is calculated only once per switching period (T_{sw}). This introduces a fixed delay equal to $T_{sw}/2$. The phase shift of the reference signal is adjusted to compensate for the known delay.

The Sine PWM implementation uses the Symmetrical PWM component. The component's **Sampling** parameter configures different means of sampling the modulation index input. With Natural sampling techniques, as is the default configuration in this controller, no delay is introduced. However, if Regular (single update at min.) or Regular (single update at max.) sampling is chosen, then a fixed delay of $T_{sw}/2$ would be introduced, similar to SV PWM. If Regular (double update) sampling is chosen, then the delay is $T_{sw}/4$.

Hysteresis PWM configuration

The Hysteresis PWM implementation is a current-controlled PWM scheme, which regulates the output current of the inverter to a reference current within a constant hysteresis band. The reference is compared with the measured output current of the inverter, “is_abc”.

3 Simulation

This model is configured to run several different experiments in order to compare the performance of each modulator.

3.1 Waveform Inspection

Each modulation scheme will impact the output waveforms. You can examine effect that different PWM methods have on the output voltage and current in the Scope labeled “VSI Waveforms”.

- Run the default simulation with Sine PWM configured and save the Scope trace with an appropriate label.
- Double click the “Controller” subsystem and change the modulation scheme to SV PWM. A new combo box field with the prompt “SVPWM modulation strategy” appears. Users can choose from the following SVPWM strategies.
 - Symmetrical
 - DPWM0
 - DPWM1
 - DPWM2
 - DPWM3
 - DPWMMIN
 - DPWMMAX

Run and save the traces to compare the current ripple on different regions of the AC waveform.

- Change the modulation scheme to Hysteresis PWM. Due to the non-periodic switching frequency inherent to hysteresis current control, the averaged waveforms of the VSI output terminal voltages will appear irregular.

3.2 Total Harmonic Distortion (THD)


Re-run each each modulator and observe the phase A THD in the Display block. You will notice that the Symmetrical SVPWM generates the lowest harmonic distortion at the output when compared to the others for the same switching frequency. Tab. 1 below highlights the THD results for each modulation strategy.

Table 1: Total Harmonic Distortion results

PWM	THD
Sine	7.24 %
SVPWM	Symmetrical 6.15 %
	DPWM0 8.22 %
	DPWM1 8.7 %
	DPWM2 8.22 %
	DPWM3 7.72 %
	DPWMMIN 8.22 %
	DPWMMAX 8.22 %
Hysteresis	8.41 %

3.3 Harmonic Spectrum Analysis

The PLECS Scope can be used to visualize the three-phase currents harmonic spectrum associated with each modulation scheme.

- Clear the previous simulation results and run the simulation with the Sine PWM configuration. If one wants also to see the harmonic components present in the voltage waveforms, the Periodic Average block must be commented through.
- The harmonics present in each waveform may be viewed by clicking the  button at the top of the Scope to view the Fourier spectrum of the signals.
- To match Fig. 2, set the **Set base frequency**: to the fundamental frequency (50 Hz), and specify 500 for the Number of Fourier Coefficients, **N**. These settings are configured so the Fourier spectrum results show the harmonics up to 25 kHz, or 2.5 times the switching frequency of 10 kHz for Sine PWM and SV PWM.
- In the **Scope Parameters**, set the **Scaling** to Absolute, linear, and zoom in on the y-axis.
- Re-run the above for each modulation scheme.

For the Sine PWM and SV PWM schemes, the dominant harmonics are centered around integer multiples of the switching frequency. Notice that with Hysteresis PWM the harmonics generated are non-periodic and have frequency content across the harmonic spectrum, as seen in Fig. 3.

3.4 Hysterersis band

One additional study to consider is the effect that the hysteresis band has on the simulation speed and waveforms.

- Double click the “Controller” subsystem and select the Hysteresis PWM configuration.
- Reduce the Hysteresis Band setting by an order of magnitude.
- Observe how the current waveform better resembles the reference current. Note that the simulation speed is impacted due to requiring of smaller time steps.

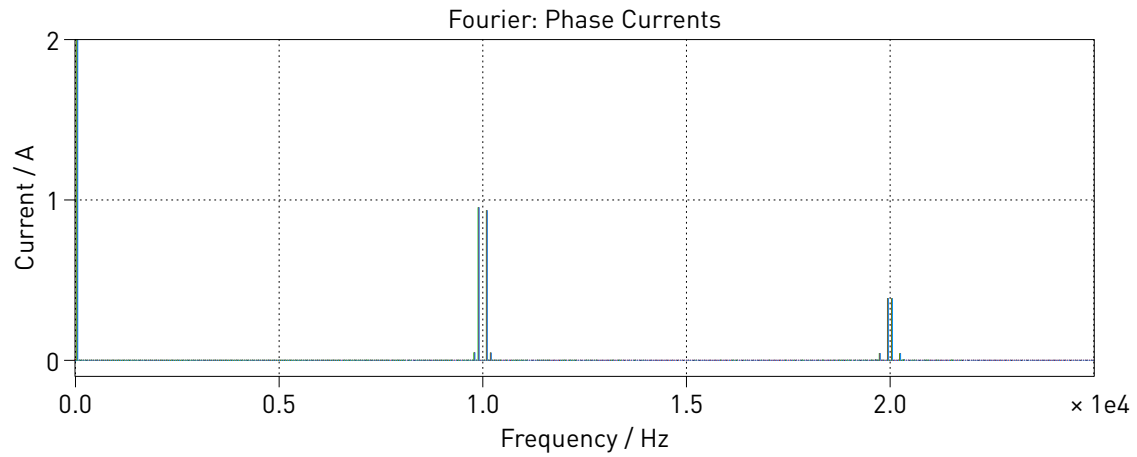


Fig. 2: Zoomed in Fourier spectrum using Sinusoidal PWM controller

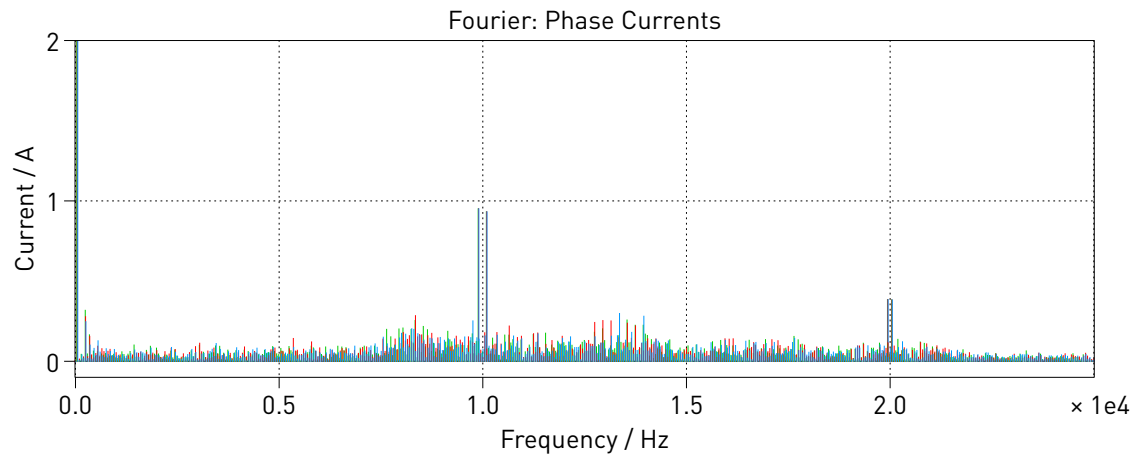


Fig. 3: Zoomed in Fourier spectrum using Hysteresis PWM controller

4 Conclusion

This model discusses the operation of an unregulated three-phase VSI and implements three major modulation techniques for its operation. The harmonics generated by each modulation strategy are compared.

Revision History:

PLECS 4.4.1	First release
PLECS 4.7.1	Use the updated library Space Vector PWM modulator block

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