



**Embedded
Code Generation**
DEMO MODEL

DC Microgrid

Microgrid with two battery storage systems, a grid interface converter, a constant power load and PV production

Last updated in C2000 TSP 1.5.1

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1 Overview

This demo model shows the simulation of a bipolar low-voltage DC microgrid. The microgrid is composed of the following main elements:

- **Two Battery Storage Systems (BSS):** Each of the two battery storage systems consists of two dual active bridges with their inputs in series and outputs in parallel. Both BSSs are controlling the bipolar DC power link voltage. Each BSS delivers a rated power of 20 kW and a switching frequency of 15 kHz. Every BSS will act as a grid-supporting converter on the microgrid. Which means that they are not only able to maintain the DC-bus voltage stable, but also to control the power flow among the two paralleled converters. To achieve this parallel operation of both BSSs, droop control is applied.
- **Grid Interface Converter (GIC):** An NPC (neutral point clamped) voltage source inverter is used as the interface between the common DC power link and the low-voltage utility AC grid. The nominal power of the inverter is 20 kW. The switching frequency was selected as 20 kHz. Since the grid interface converter is power controlled, it acts as a constant power load on the common DC power link.
- **Constant power loads (CPL):** A simplified model of a constant power load is implemented by means of a voltage controlled current source with limited bandwidth. The power drawn by the load is variable and can be changed during the simulation.
- **PV production:** PV production is emulated by a controlled current source. The installed peak power can be adjusted freely during simulation.

This document provides an explanation of the typical workflow of the PLECS Embedded Coder using Texas Instruments (TI) C2000 MCUs. Combined with a PLECS RT Box, the performance of the MCU can be verified directly. The entire DC microgrid model runs on a total of 4 RT Boxes.

Note This model contains model initialization commands that are accessible from:

PLECS Standalone: The menu **Simulation + Simulation Parameters... + Initializations**

PLECS Blockset: Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

2 Model

A microgrid is a local electrical energy grid that interconnects loads, storage and generation within a clearly defined electrical boundary and that acts as a single controllable entity with respect to the mains utility AC grid. Such a microgrid can either operate under grid-connected or islanded mode. Under grid-connected operation the microgrid can exchange energy in a controlled way with the mains AC grid. In islanded mode the microgrid is disconnected from the utility grid and has to feed all loads independently. The common power feeder of a microgrid can either be AC or DC. In this demo model there is a DC common power feeder and the microgrid can operate in grid-connected and islanded mode. The voltage level of the common DC-bus is ± 375 V.

The model is composed of different subsystems. Hereafter a short overview is given for each subsystem:

- **DC Power Grid:** This subsystem includes the passive structure of the DC microgrid. The different power electronics converters are interconnected by a parasitic line impedance. Additionally, PV production and a constant power load (CPL) are emulated in this subsystem.
- **BSS1 plant:** This subsystem includes the power circuit of the first battery storage system. Each BSS consists of two dual active bridges with their input sides in series and the output sides connected in parallel. The same is true for the subsystem “BSS2 plant”.

The diagram illustrates the power electronics system architecture, divided into three main sections: BSS1, BSS2, and GIC.

- BSS1 and BSS2 Sections:** Each section consists of a controller (BSS1/BSS2 Controller) and a plant (BSS1/BSS2 plant). The controllers receive feedback signals from the plants via ADCs (z⁻¹ block). The plants receive PWM signals from the controllers and output various signals (V_{LV}, V_{HV}, I_{LV}, I_{HV1}, I_{LV1}, V_{C1}, V_{C2}) to the DC Power Grid. The plants also output status signals (Tz_i, En_i, Tz_o, En_o, LED Blinking, Powerstage enabled, Trip zone deactivated) to the SFP (Signal Processing Function) blocks.
- GIC Section:** The GIC (Grid Interfacing Controller) consists of a GIC Controller and a GIC plant. The controller receives feedback signals from the plant via ADCs (ADC A, ADC B, ADC C). The plant receives PWM signals from the controller and outputs various signals (I_g, V_g, V_{mid}, V_{dc}) to the DC Power Grid. The plant also outputs status signals (LED 29: Switching Enabled, LED 31: Blinking, Enable Inverter (MCU)) to the SFP (Signal Processing Function) blocks.
- DC Power Grid:** The DC Power Grid is represented by a vertical line on the left. It receives signals from the BSS1 and BSS2 plants and outputs signals to the SFP blocks. The SFP blocks are labeled SFP A Out, SFP A In, SFP B Out, SFP B In, SFP C Out, and SFP C In.
- ADC Signal mapping (offline only):** A block on the right shows the mapping of ADC signals to the GIC plant. It includes inputs for I_g, V_g, V_{mid}, and V_{dc}, and outputs for ADC A, ADC B, and ADC C.

2.1 DC Power Grid

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4. m1

→ > 650



$$I_{CPL} = \frac{P_{ref}}{V_{dc}} \frac{1}{\frac{1}{\omega_c} s + 1}$$

The first-order low-pass filter represents the bandwidth of the current loop controller of the emulated power electronics converter. The cut-off frequency ω_c can be adjusted in the mask dialog of the CPL subsystem.

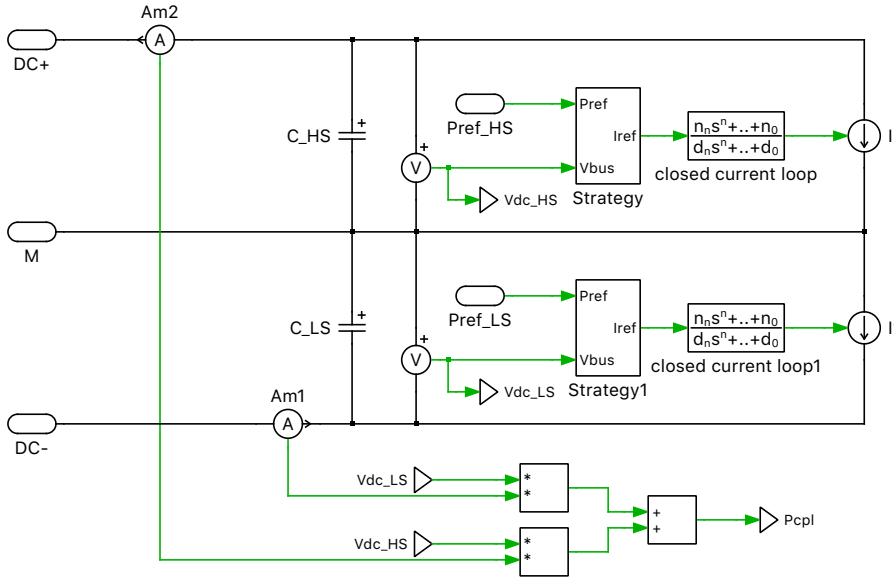


Figure 4: Implementation of the constant power load

2.2 BSS1 and BSS2 plant

Two battery storage systems are connected to the common DC power link. Each power circuit includes a DC-DC converter based on an Input-Series/Output-Parallel Dual Active Bridge (DAB) structure. The input-side (series connection) is connected to the common DC power link, the output-side (parallel connection) interfaces with an electrochemical battery. In order to smooth the power delivered to the battery, an additional filter stage is connected in-between the battery and DAB output. The implementation of the BSS subsystems is given in Fig. 5.

2.3 BSS1 and BSS2 Controllers

The subsystem “BSS Controller” contains the control algorithms for the two BSSs.

Target Blocks

The implementation contains ADC and PWM blocks from the TI C2000 target component library. The measurement of the bipolar DC-link voltages, battery-side voltage and the individual battery-side currents are introduced to the model environment using the ADC blocks from the TI C2000 component library. In order to convert the detected analog voltage into values with physical units to be used by the control algorithm, a scaling factor and an offset are provided for each channel via the parameter window of the ADC block. The ADC unit and the analog input channel parameters can be modified accordingly per available resources of different MCUs.

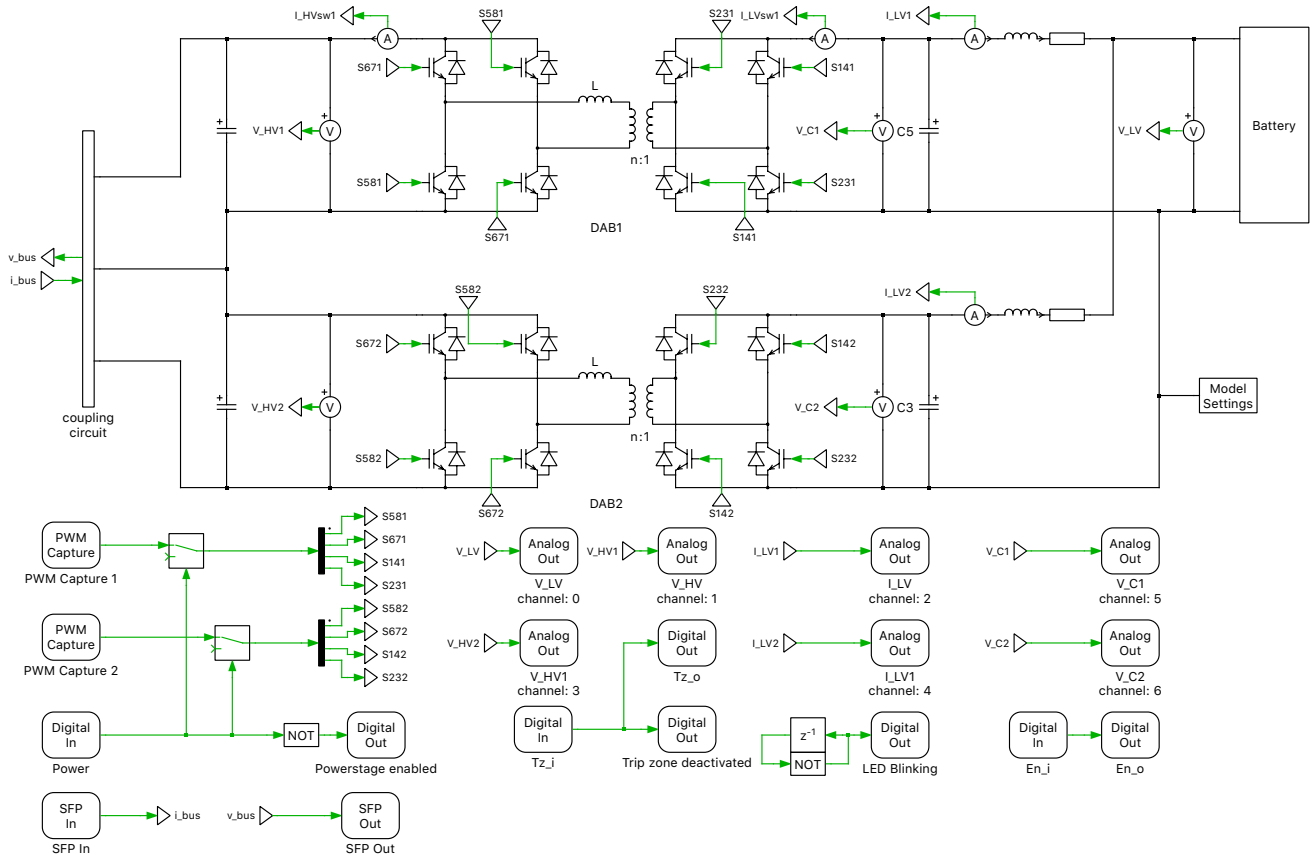


Figure 5: The implementation of the BSS subsystems

Droop Control

The two battery storage systems are paralleled and both control the DC-bus voltage. Paralleling converters offers advantages compared to one single high-power converter, such as increased reliability, maintenance under operation and reduced stress on power components. The main challenge of paralleled converters is to achieve load current sharing between the converters and to eliminate current sharing mismatch. To achieve accurate load sharing among the paralleled converters, special control techniques have to be implemented. One simple method is introducing a virtual series resistance in the control loop, i.e. droop-control.

The droop controller compares the voltage reference against the measured voltage on the output capacitor. The difference is amplified by a gain, the so-called droop-gain. Selecting an appropriate droop-gain K_{droop} is always a compromise between current sharing accuracy and allowed voltage deviation, as shown in [1]. The higher the droop gain, the smaller the voltage deviation. The smaller the droop gain, the higher the current sharing accuracy.

$$I_{\text{BSS}}^* = K_{\text{droop}}(V^* - V_{\text{meas}})$$

Cascaded Current and Voltage Control

The calculated reference current I_{BSS}^* is an input to the current loop. This outer current loop regulates the current in the filter inductor and provides a voltage reference for the inner voltage controller. Finally, this inner voltage controller provides a current reference which is used to calculate the required phase-shift φ between the primary and secondary full-bridge.

To achieve a controlled ramping of the DC-bus voltage during startup-up, a simple finite state machine is implemented. If the total DC-bus voltage is below 750 V at the start-up process, the droop controller

is bypassed and a constant current reference of 5 A is applied to the outer current loop to build up the DC voltage. Feeding a constant current into a capacitor leads to ramp up of the voltage on a capacitor.

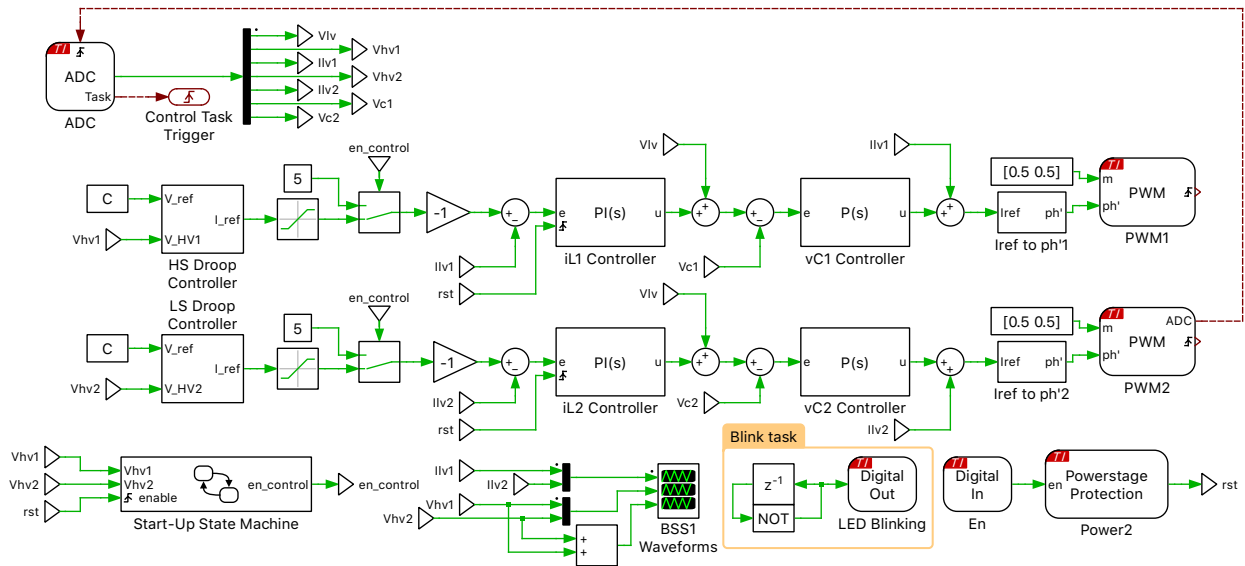


Figure 6: Controller implementation of the two BSSs

2.4 GIC plant

The twelve PWM switching signals are sensed by three PWM Capture blocks from the RT Box target support library. The measurements of the DC voltages, AC currents and AC voltages interface with the connected controllers via Analog Out ports. A Digital Out block labeled “Enable Inverter (MCU)” forwards the external digital input signal to a digital output pin of the RT Box. This pin is connected to a GPIO of the MCU to enable/disable PWM outputs via a finite state machine implemented in control software. The mechanism of the MCU’s PWM enable/disable function will be elaborated in Section 3.

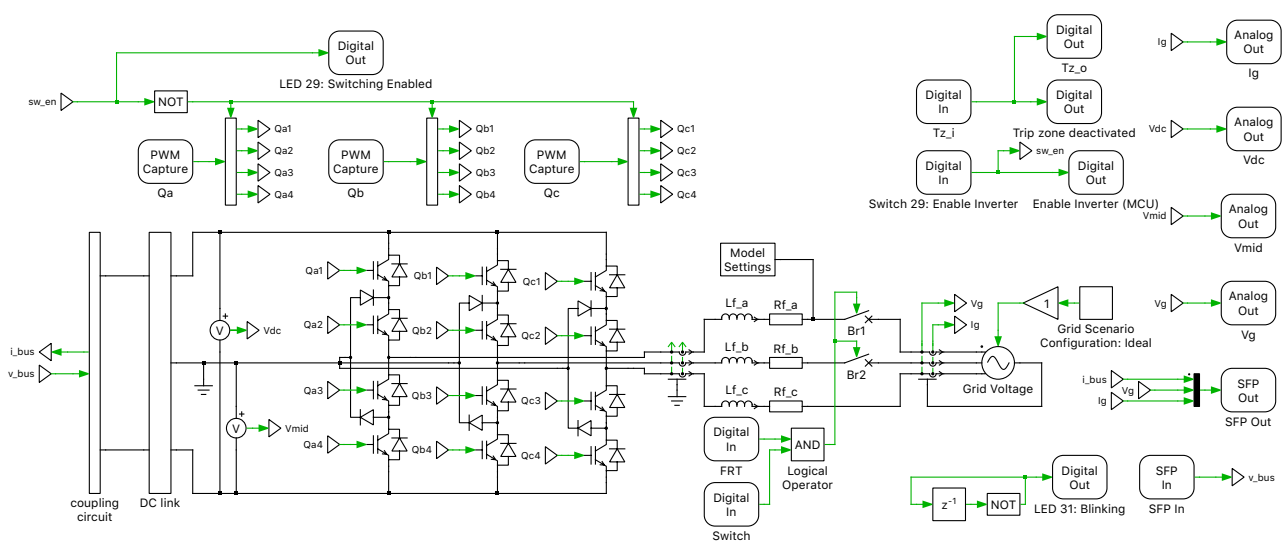


Figure 7: Implementation of the GIC subsystem

condition. In addition a global enable has to be given to the controller with a dip-switch connected to an digital input of the MCU.

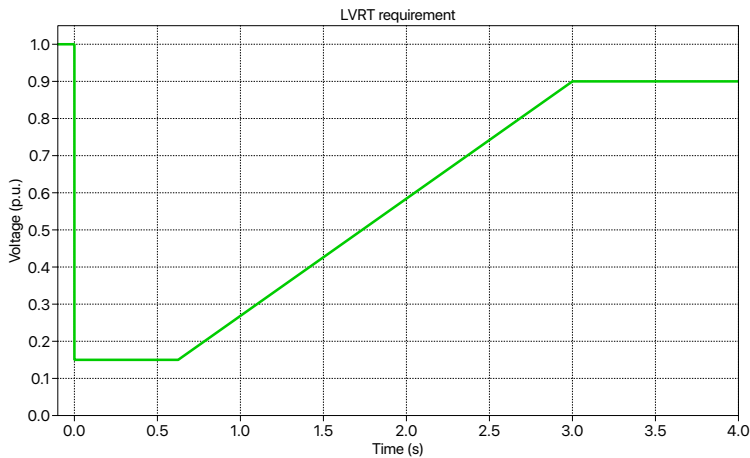


Figure 9: The low voltage ride through requirement, above the limit the generation unit has to stay connected, below the limit it may disconnect from the AC grid.

2.6 Coupling Circuit

The entire DC microgrid model runs on a total of 4 RT Boxes. Therefore, the model has to be divided into smaller portions to optimize the execution time on the individual RT Boxes. The circuit is divided by using a coupling circuit as shown in Fig. 10. This model partitioning has to be done at strategic points of the circuit in order to not reduce the stability margins of the model, e.g. next to a capacitor where the voltage rate of change is limited or next to an inductor where the same is true for the current. As one can see in Fig. 10, the measured current on “Box A” is transferred over SFP to “Box B” and delivers the control signal for the two controlled current sources. The same process can be observed with the measured voltage signals on “Box B”. This coupling circuit, which can be seen as an ideal gyrator with unity gain, enables to split the complex DC microgrid model into smaller pieces, which can be simulated on individual RT Boxes. The left part of the coupling circuit is implemented

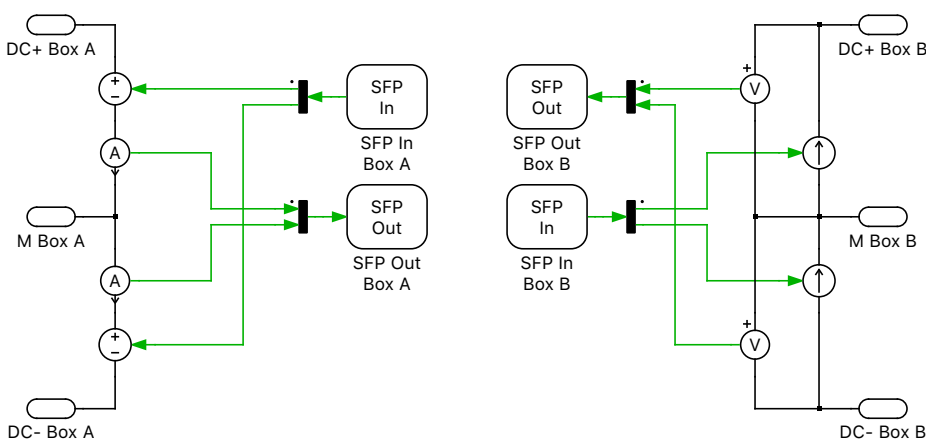


Figure 10: Coupling circuit used to split a circuit among different RT Boxes.

on one RT Box, the right part on a second one. Each converter is connected to the central “DC Power Grid” model by using such a coupling circuit.

3 Simulation

In addition to running a simulation of this demo model in offline mode on a computer, each of the subsystems can be deployed on a real target by using the PLECS Coder. The CPL and PV system represent the dynamic load and generation profiles of the microgrid. Two BSSs coordinate to regulate the DC link voltage as it changes in response to the net power balance of the load and generation. The GIC supplies a constant 5kW into the AC grid unless a grid fault is detected. If an AC line fault is detected, the GIC controller electrically isolates the DC Microgrid from the AC system, until the fault conditions have elapsed.

Due to the complexity of the model, it has to be split onto 4 PLECS RT Boxes for the HIL verification. Each “plant” subsystem is running on a different RT Box. The RT Box running the “DC Power Grid” subsystems acts as the master for startup. All other RT Boxes act as a slave and synchronize their startup on SFP port A. A schematic overview of the hardware setup is shown in Fig. 11.

3.1 Hardware Setup

The following material is needed to setup a HIL simulation of the DC microgrid model:

- 4x PLECS RT Box 1
- 3x SFP cables
- 3x RT Box LaunchPad Interface
- 2x TI 28069M LaunchPad (for the two BSS controllers)
- 1x TI 28379D LaunchPad (for the GIC controller)

To set up the HIL simulation you have to execute the following steps.

- 1** Stack 4 PLECS RT Boxes vertically, labeled as “DC Power Grid”, “BSS1 plant”, “BSS2 plant” and “GIC plant”.
- 2** Connect the SFP cable from the **A**, **B** and **C** ports of the “DC Power Grid” box to the **A** port of the other three boxes, respectively.
- 3** Connect the three RT Box LaunchPad Interface boards to the boxes named “BSS1 plant”, “BSS2 plant” and “GIC plant”. Change the position of all switches in the three interface boards to the position away from the RT Boxes.
- 4** Plug the corresponding LaunchPad to each interface board (TI 28069M LaunchPad for “BSS1 plant” and “BSS2 plant”, TI 28379D LaunchPad for “GIC plant”)
- 5** Download the four plant subsystems to the RT Boxes and the three controller subsystems to the LaunchPads (in arbitrary order).
- 6** After system start (blue LED of all four boxes continuously on), change the position of the “DI28” and “DI29” switch of the interface board of the “BSS1 plant” and/or “BSS2 plant” RT Box pointing towards the RT Box. One of the two (or both) BSS will now start to build up the voltage of the DC-bus.
- 7** Change the “DI28” and “DI29” switch of the “GIC plant” interface board in the position pointing to the RT Box.
- 8** Now, the DC microgrid is running on the four RT Boxes. The three converters are controlled by the three LaunchPads plugged on the interface boards.

Four RT Boxes are stacked to emulate the DC microgrid system that includes a grid interlinking converter, two battery storage systems, a PV production and a constant power load. Different scenarios can be simulated in this microgrid setup:

- AC grid fault scenarios: The GIC is connected to special implementation of a three-phase voltage source. This voltage source enables testing the controller response to abnormal grid conditions, e.g. voltage disturbances, frequency disturbances and changes in the phase-angles. In this demo only

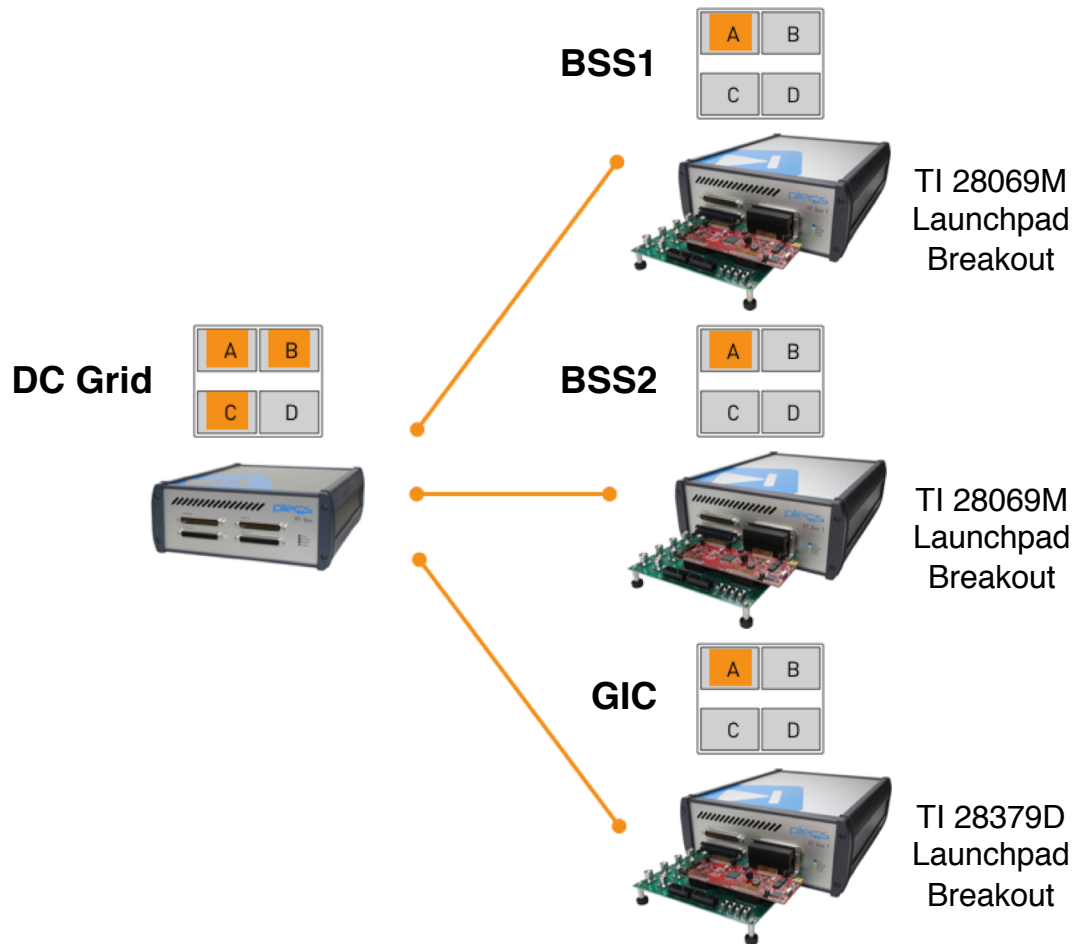


Figure 11: Hardware setup of the HIL verification

undervoltage events are considered. If you set the Gain block to a value between 0 and 1, the GIC will ride through the fault according to the clearing time depicted in Fig. 9.

- Switch off one BSS: During normal operation, the DC-bus voltage is maintained by two BSSs working in parallel. However, a fault in one BSS can be simulated. This can be done by changing the “DI29” switch of one of the two BSS Launchpad interface boards in the direction away from the RT Box. By doing this, one BSS will stop its operation and the remaining BSS has to take over the whole power needed to balance the DC microgrid.
- The dynamic of the PV production and the CPL can be changed prior to a simulation by changing the variable `DCgrid.plant.time_scaling` in the **Initialization commands** of the model.

The transient results of the simulation can be observed and evaluated using the PLECS Scopes when the **External Mode** is connected.

3.2 Results

The main offline simulation results are shown in Fig. 12. The DC-bus voltage is build up from zero at simulation start. For this, both battery storage systems feed a constant current into the DC-bus. Once the DC-bus voltage reaches 750 V, the controller is switched into droop control and both BSSs control the bus voltage towards 750 V. At around $t = 0.2$ s, the grid interface converter starts to inject a constant power of 5 kW into the AC grid. Also the PV production and the constant power load feed or load the common DC-bus with a variable power level. To achieve voltage control on the DC-bus the

two BSSs have to balance the power on the DC power link. This can be summarized as the difference between the total power generation and the total load on the DC-bus:

$$P_{BSS} = P_{PV} - P_{CPL} - P_{GIC}$$

Since both BSSs work in parallel, the power P_{BSS} is distributed on both converters. Even though the droop gain is the same for both BSSs, there is a difference in the power level of the two individual BSS. This can also be observed in Fig. 12. This mismatch is due to the uneven values of the resistive part of the coupling impedance between the converters and the DC-bus.

At $t = 0.5$ s, the AC grid voltage sags down to 0 p.u. Due to this, the GIC-controller stops immediately the switching operation of the AC/DC inverter. Also the circuit breaker between inverter and AC grid is opened. At $t = 0.8$ s, the AC grid voltage is restored back to 1 p.u. This triggers the reconnection of the inverter. Once the PLL is re-locked to the grid voltage, the GIC starts again to inject the power into the AC grid.

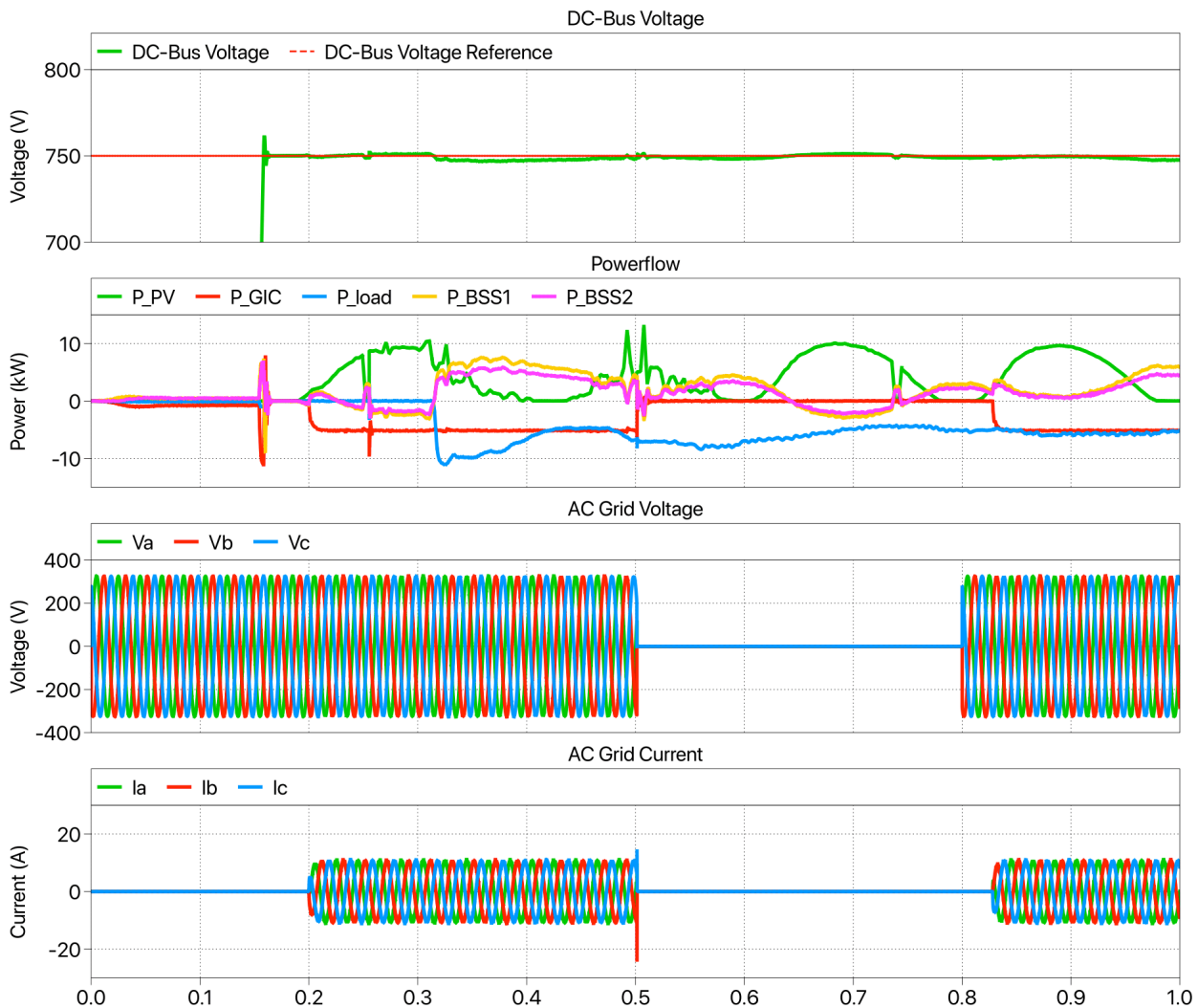


Figure 12: The figure caption of the simulation results

4 Conclusion

This model demonstrates the simulation of an entire DC microgrid that supports embedded code generation for TI C2000 MCUs. The hardware of the test system comprises 4 RT Boxes to simulate the

different physical parts of the overall power system and 3 TI Launchpads to implement the local control units of the converters. The whole offline and real-time deployment can be done from one single PLECS model as well as the monitoring of simulation results and real-time operation. Further development on this comprehensive microgrid model may include additional power loads and sources as well as a supervisory/centralized controller that communicates to the local control units of each converter.

References

- [1] GAO, F., KANG, R., CAO, J. et al., *Primary and secondary control in DC microgrids: a review.*, J. Mod. Power Syst. Clean Energy 7, 2019, 227-242. [Online]. Available: <https://link.springer.com/article/10.1007/s40565-018-0466-5>.

Revision History:

C2000 TSP 1.1.1	First release
C2000 TSP 1.4.5	Updated the powerstage protection parameters, Updated the web links
C2000 TSP 1.5.1	Minimized the usage of double-precision math in the controller; Set the Sync to "Self" on PWM2

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