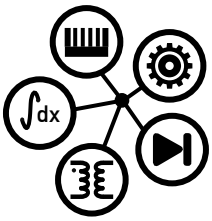

RT Box

DEMO MODEL

Three-level Grid-connected NPC Solar Inverter with LCL-filter and Active Damping

Last updated in RT Box Target Support Package 3.0.3

www.plexim.com

- Request a PLECS and PLECS Coder trial license
- Get the latest RT Box Target Support Package
- Check the PLECS and RT Box documentation

1 Overview

This RT Box demo model features a grid-connected three-level neutral-point clamped (NPC) inverter with closed-loop control using a space-vector pulse-width modulation (SVPWM) scheme. This demo model has the following features:

- The plant and controller models are implemented inside one subsystem. This allows a complete transient offline simulation in PLECS, as well as a real-time simulation of both controller and plant model.
- The inverter delivers $50\,\mathrm{kW}$ from an $800\,\mathrm{V}$ DC input to a $50\,\mathrm{Hz}$, $230\,\mathrm{V_{rms}}$ stiff grid. The link between the inverter and the stiff grid features an LCL-filter. The resonance brought by the LCL-filter may lead to controller instability, thus some damping technique is needed to suppress this resonance peak. In this demo model, an active damping technique is employed over passive damping, with the merit of less power losses.

This document describes the implementation of the power stage and controls using the PLECS Electrical and Control domains. It presents the current control and modulation with a special focus on the three-level SVPWM technique, and the necessary neutral-point balancing algorithm is also included.

The execution time represents the actual time it takes to execute one calculation step of the PLECS model on the RT Box hardware. The chosen discretization step sizes and average execution times for each core on the RT Box are shown in Tab. 1.

Table 1: Discretization step size and average execution time of the demo on one RT Box

	Core 0: exec. time / step size	Core 1: exec. time / step size	FPGA step size
RT Box 2 or 3	$2.8\,\mu s$ / $5\,\mu s$	$1.8\,\mu s$ / $50\,\mu s$	$556\,ns$
RT Box 1	$6.5\,\mu s$ / $10\,\mu s$	N/A	N/A

1.1 Requirements

To run this demo model, the following items are needed (available at `www.plexim.com`):

- One PLECS RT Box and one PLECS Coder license
- The RT Box Target Support Package
- Follow the step-by-step instructions on configuring PLECS and the RT Box in the Quick Start guide of the RT Box User Manual.
- Two 37 pin Sub-D cables to connect the box in loop-back setup at the front panel.

Note that this demo model is primarily showcasing the `multi-tasking` mode, which can run on an RT Box 1, 2 or 3.

Note RT Box CE cannot be used as the Controller box in this demo due to its reduced amount of analog input channels.

- When the target is an RT Box 2 or 3, the main CPU core (Core 0) runs the plant as “Base task” with a sample time of `Ts_plant`. Another core (Core 1) runs closed-loop controls in “Controller” task in parallel with a sample time of `Ts_controller`, which is much slower and usually equals the switching period of the converter. In this way, the multi-core feature of the RT Box 2 or 3 is showcased by splitting the computational effort onto different cores. Besides, the setup can easily transition to a HIL or RCP test later on.

- However if the user has only a single RT Box 1 available, this model can also run with the multi-tasking feature onto the only CPU core of the RT Box 1, but in a pre-emptive multi-tasking fashion. In this case, the “Base task” is doing the plant calculation with the highest priority with a sample time of `Ts_plant`. The “Controller” task is executed as a background task with lower priority at the sample time of `Ts_controller`.

Please check the setting under **Scheduling** tab of the **Coder options...** window.

Note This model contains model initialization commands that are accessible from:
PLECS Standalone: The menu **Simulation + Simulation Parameters... + Initializations**
PLECS Blockset: Right click in the **Simulink model window + Model Properties + Callbacks + InitFcn***

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2 Model

The top-level schematic of the demo model is depicted in Fig. 1, and it is composed of one subsystem: “Plant + Controller”. To run the model on an RT Box, the subsystem has to be configured as **atomic units** and enabled for **code generation** by right-clicking on the subsystem and choosing **Subsystem + Execution settings...**

A Delay block (z^{-1}) with a sample time equal to one controller task step is added to the offline simulation before the analog input of the controller subsystem. This emulates the calculation time delay of one control step in the real-time application.

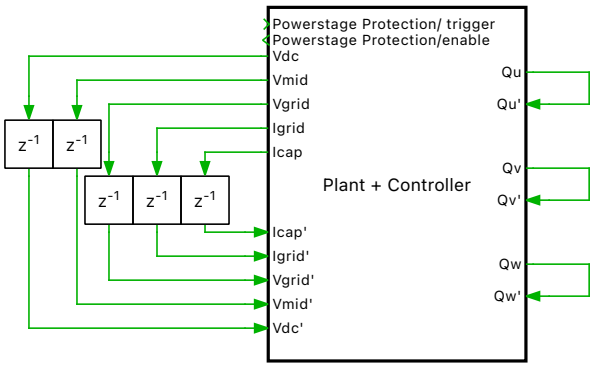


Figure 1: Top-level schematic of the three-level NPC inverter model

2.1 Three-Level NPC Inverter with LCL-Filter and Active Damping

Fig. 2 shows the circuit model of the plant, which comprises a three-level NPC inverter connected to the grid through an LCL-filter.

- **DC input**: The DC input is modeled with a simplified photovoltaic (PV) panel model. The block input is the relative solar intensity level (nominal value of 1) set by the Constant block “Sun”. The PV panel output is the intensity level multiplied with a fixed DC voltage of $800\,\mathrm{V}$.
- **Upper and lower half DC capacitors**: The upper and lower half DC capacitors have the same $1.1\,\mathrm{mF}$ capacitance value, however, in order to see the effect of the neutral-point balancing algorithm, different initial voltage values are set. Later in the real-time simulation result in section 3, one can see that the upper and lower half DC capacitors, with initial voltages of $450\,\mathrm{V}$ and $350\,\mathrm{V}$, respectively, settle at a balanced $400\,\mathrm{V}$ and $400\,\mathrm{V}$. The neutral-point balancing algorithm is further discussed in section 2.2.

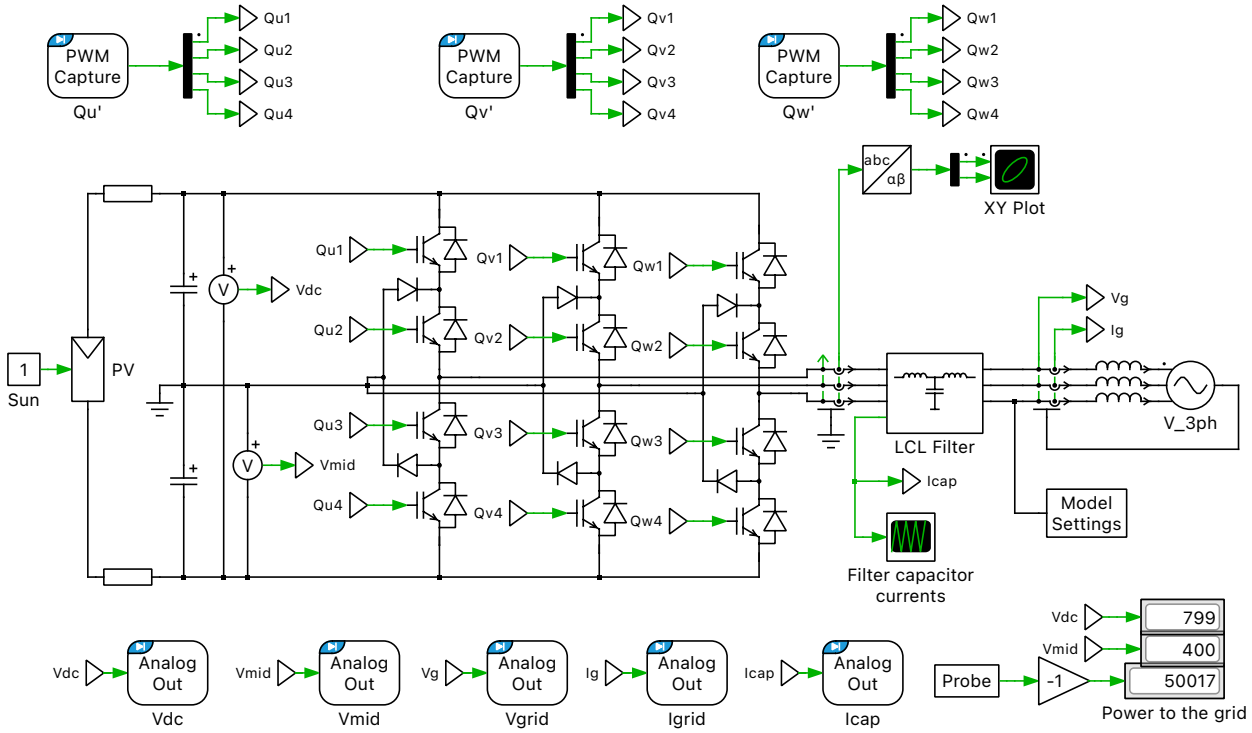


Figure 2: Schematic of the grid-connected three-level NPC inverter with LCL-filter and active damping

- **Three-level NPC inverter**: The IGBT 3-Level Half Bridge power modules from the PLECS component library are used to build up the NPC inverter topology. The modules use the sub-cycle average configuration together with the PWM Capture blocks. This ensures that incoming switching signals are sampled with high resolution, and subsequently physical states are properly calculated. This configuration is able to run online in real-time, as well as offline with a variable-step solver.

The plant model uses different blocks from the RT Box Target Support Library to access the physical input and output ports of the RT Box: the PWM Capture and Analog Output blocks, respectively. A generic description of these blocks is given in the RT Box Target Support package documentation or the "Boost Converter" RT Box demo model.

LCL-filter design

Due to the pulsating voltage at the three-level inverter output nodes, some kind of filter has to be inserted between the inverter and the grid to attenuate the switching harmonics. The filter is usually composed of inductors and capacitors, which allow the inverter to exchange active and reactive power with the grid by means of inverter control. The design guideline of the LCL-filter used here follows reference [1].

Filter capacitor C_f design To design C_f we have to consider reactive power variations due to the LCL-filter. The design base values can be defined as:

$$Z_\mathrm{b} = \frac{V_\mathrm{LL}^2}{P_\mathrm{n}}, C_\mathrm{b} = \frac{1}{\omega_\mathrm{g} Z_\mathrm{b}}, L_\mathrm{b} = \frac{Z_\mathrm{b}}{\omega_\mathrm{g}},$$

where V_LL^2 is grid line-to-line RMS voltage, P_n is the rated active power, and $\omega_\mathrm{g} = 2\pi f_\mathrm{g}$ is the grid angular frequency. Filter capacitance is related to the base value C_b as a percentage of it. Setting the maximum power variation seen by the grid as 5% (empirical value 1% - 5%), we can obtain:

$$C_\mathrm{f} = 0.05 C_\mathrm{b}$$

Filter inductors L_c and L_g design At low frequencies the LCL-filter behaves like an inductor with the total inductance of:

$$L_{dc} = L_c + L_g$$

Note that the current through filter capacitors C_f is negligible compared to that of the filter inductors. There is a relation between L_c and L_g that minimizes the voltage drop at the fundamental frequency and maximizes filtering ability. If we express L_c and L_g as a percentage of L_{dc} with $\alpha \in [0, 1]$, then:

$$L_c = \alpha L_{dc}, L_g = (1-\alpha)L_{dc}$$

Since the LCL resonant circuit consists of L_c, C_f, and L_g all in parallel, the LCL resonant frequency is:

$$\omega_r = \sqrt{\frac{L_c + L_g}{L_c C_f L_g}}$$

Therefore the equivalent inductance L_{eq} that sets the resonant frequency can be defined as L_c and L_g in parallel:

$$L_{eq} = \frac{L_c L_g}{L_c + L_g} = \alpha(1-\alpha)L_{dc}$$

The minimum L_{eq} is achieved when $L_c = L_g = 0.5L_{dc}$. By choosing L_{dc} to be 10% (empirical value) of the base value L_b, L_c and L_g are easily determined:

$$L_c = L_g = 0.05L_b$$

Active damping technique using filter capacitor currents

To suppress the high peak gain at the LCL resonant frequency, a damping resistor for the input filter can be placed as a passive damping method [2]. Passive damping is a simple approach but introduces additional losses, while active damping solves the problem through a control modification with a virtual resistor which is lossless.

Fig. 3 depicts the single-phase equivalent ideal LCL-filter and its corresponding block diagram [1]. Fig. 4 demonstrates the case of a damped filter, where the damping resistor is placed in series with the filter capacitor [1]. The block diagram in Fig. 4 shows that with a virtual gain component (emulating "RD" in Fig. 4) the same damping effect can be added to the control scheme of an ideal LCL-filter while removing the power losses of the physical damping resistor. For the active damping approach, filter capacitor currents have to be measured, which requires three (or only two for the case of balanced three-phase currents) additional analog in-/outputs. The filter in Fig. 3 can be described with the state equa-

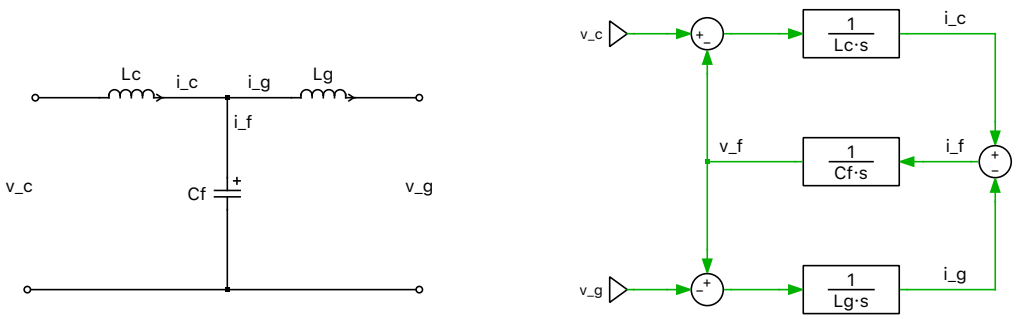


Figure 3: Single-phase equivalent ideal LCL-filter and corresponding block diagram

tions in the s-domain:

$$v_c(s) = sL_c i_c(s) + v_f(s)$$

$$v_g(s) = v_f(s) - sL_g i_g(s)$$

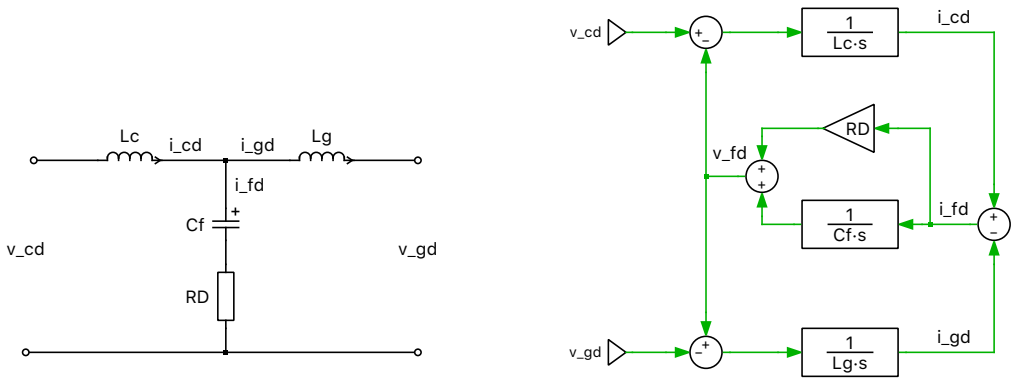


Figure 4: Single-phase equivalent damped LCL-filter and model, damping resistor in series with capacitor

$$v_{\mathrm{f}}(s) = \frac{i_{\mathrm{f}}(s)}{sC_{\mathrm{f}}}$$

$$i_{\mathrm{c}}(s) = i_{\mathrm{f}}(s) + i_{\mathrm{g}}(s)$$

The voltage and current transfer functions of the ideal LCL-filter are therefore:

$$H_{\mathrm{v_f}}(s) = \frac{v_{\mathrm{f}}(s)}{v_{\mathrm{c}}(s)} = \frac{1}{L_{\mathrm{c}}C_{\mathrm{f}}}\frac{1}{s^2+\omega_{\mathrm{r}}^2}$$

$$H_{\mathrm{i_f}}(s) = \frac{i_{\mathrm{f}}(s)}{v_{\mathrm{c}}(s)} = \frac{i_{\mathrm{f}}(s)}{v_{\mathrm{f}}(s)}\frac{v_{\mathrm{f}}(s)}{v_{\mathrm{c}}(s)} = \frac{1}{L_{\mathrm{c}}}\frac{s}{s^2+\omega_{\mathrm{r}}^2}$$

where ω_{r} is the resonant frequency defined before.
For the LCL-filter with damping resistance in Fig. 4 we have:

$$v_{\mathrm{c}}^d(s) = s\cdot L_{\mathrm{c}}\cdot i_{\mathrm{c}}^d(s) + v_{\mathrm{f}}^d(s)$$

$$v_{\mathrm{g}}^d(s) = v_{\mathrm{f}}^d(s) - s\cdot L_{\mathrm{g}}\cdot i_{\mathrm{g}}^d(s)$$

$$v_{\mathrm{f}}^d(s) = i_{\mathrm{f}}^d(s)\left(R_{\mathrm{D}} + \frac{1}{sC_{\mathrm{f}}}\right)$$

$$i_{\mathrm{c}}^d(s) = i_{\mathrm{f}}^d(s) + i_{\mathrm{g}}^d(s)$$

The damping resistor R_{D} is often selected as one third of the impedance of the filter capacitor C_{f} at resonant frequency [1]:

$$R_{\mathrm{D}} = \frac{1}{3\omega_{\mathrm{r}}C_{\mathrm{f}}}$$

Therefore we can derive the same voltage and current transfer functions of interest:

$$H_{\mathrm{v_f}}^d(s) = \frac{v_{\mathrm{f}}^d(s)}{v_{\mathrm{c}}^d(s)} = \frac{1}{L_{\mathrm{c}}C_{\mathrm{f}}}\frac{1+sR_{\mathrm{D}}C_{\mathrm{f}}}{s^2+\omega_{\mathrm{r}}^2(1+sR_{\mathrm{D}}C_{\mathrm{f}})}$$

$$H_{\mathrm{i_f}}^d(s) = \frac{i_{\mathrm{f}}^d(s)}{v_{\mathrm{c}}^d(s)} = \frac{i_{\mathrm{f}}^d(s)}{v_{\mathrm{f}}^d(s)}\frac{v_{\mathrm{f}}^d(s)}{v_{\mathrm{c}}^d(s)} = \frac{1}{L_{\mathrm{c}}}\frac{s}{s^2+\omega_{\mathrm{r}}^2(1+sR_{\mathrm{D}}C_{\mathrm{f}})}$$

For the case without damping resistance, we define:

$$H_{\mathrm{v_f}}(s) = \frac{v_{\mathrm{f}}(s)}{v_{\mathrm{c}}(s)} = \frac{L_{\mathrm{g}}}{s^2L_{\mathrm{c}}C_{\mathrm{f}}L_{\mathrm{g}} + L_{\mathrm{c}} + L_{\mathrm{g}}} = H_1(s)$$

$$\frac{i_{\mathrm{f}}(s)}{v_{\mathrm{f}}(s)} = sC_{\mathrm{f}} = H_2(s)$$

For the case with damping resistance, we define:

$$H^d_{\mathrm{v_f}}(s) = \frac{v^d_{\mathrm{f}}(s)}{v^d_{\mathrm{c}}(s)} = \frac{L_{\mathrm{g}}(1 + sR_{\mathrm{D}}C_{\mathrm{f}})}{s^2L_{\mathrm{c}}C_{\mathrm{f}}L_{\mathrm{g}} + (L_{\mathrm{c}} + L_{\mathrm{g}})(1 + sR_{\mathrm{D}}C_{\mathrm{f}})} = H_3(s)$$

For the active damping technique, we would like to achieve $H_3(s)$ without a physical R_{D}, but rather with a virtual resistor with the value of R_{D}. Fig. 5 shows the block diagram of the active damping control loop with the gain of K_{AD}. We want the closed-loop transfer function in Fig. 5 to be similar to $H_3(s)$.

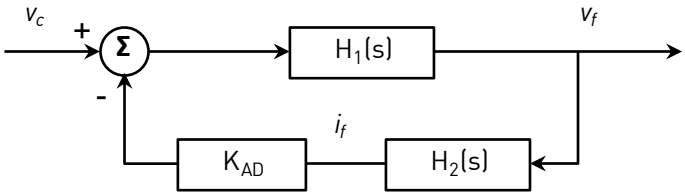


Figure 5: Active damping control loop block diagram with capacitor voltage/current as feedback

Thus in Fig. 5,

$$H_{\mathrm{CL}}(s) = \frac{H_1(s)}{1 + H_1(s)H_2(s)K_{\mathrm{AD}}} = \frac{\frac{L_{\mathrm{g}}}{s^2L_{\mathrm{c}}C_{\mathrm{f}}L_{\mathrm{g}}+L_{\mathrm{c}}+L_{\mathrm{g}}}}{1 + \frac{L_{\mathrm{g}}}{s^2L_{\mathrm{c}}C_{\mathrm{f}}L_{\mathrm{g}}+L_{\mathrm{c}}+L_{\mathrm{g}}}sC_{\mathrm{f}}K_{\mathrm{AD}}} = \frac{L_{\mathrm{g}}}{s^2L_{\mathrm{c}}C_{\mathrm{f}}L_{\mathrm{g}} + L_{\mathrm{c}} + L_{\mathrm{g}} + sL_{\mathrm{g}}C_{\mathrm{f}}K_{\mathrm{AD}}}$$

And with K_{AD} selected as:

$$K_{\mathrm{AD}} = \frac{L_{\mathrm{c}} + L_{\mathrm{g}}}{L_{\mathrm{g}}}R_{\mathrm{D}}$$

we have

$$H_{\mathrm{CL}}(s) = \frac{L_{\mathrm{g}}}{s^2L_{\mathrm{c}}C_{\mathrm{f}}L_{\mathrm{g}} + L_{\mathrm{c}} + L_{\mathrm{g}} + sL_{\mathrm{g}}C_{\mathrm{f}}\frac{L_{\mathrm{c}}+L_{\mathrm{g}}}{L_{\mathrm{g}}}R_{\mathrm{D}}} = \frac{L_{\mathrm{g}}}{s^2L_{\mathrm{c}}C_{\mathrm{f}}L_{\mathrm{g}} + (L_{\mathrm{c}} + L_{\mathrm{g}})(1 + sR_{\mathrm{D}}C_{\mathrm{f}})}$$

This final $H_{\mathrm{CL}}(s)$ is close enough to $H_3(s)$ that we can neglect the term "$R_{\mathrm{D}}C_{\mathrm{f}}$" in the numerator of $H_3(s)$ since it is much smaller than 1. Note that the implementation should be considered for both axis regulator for i_{d} and i_{q}. This virtual damping gain K_{AD} is located inside the controller subsystem (see later Fig. 6) as the Gain block "Virtual damping resistor".

2.2 Three-Level Space-Vector Pulse-Width Modulation Scheme and Controls

The controller subsystem including measurement transformation, three-level SVPWM and closed-loop dq current controller are captured in Fig. 6. It contains Analog In and PWM Out blocks from the RT Box Target Support library. A generic description of these blocks is given in the RT Box Target Support package documentation or the "Boost Converter" RT Box demo model.

The i_{d} and i_{q} current controllers are designed using the Magnitude Optimum Criterion based on the following transfer function:

$$H_{\mathrm{OL}}(s) \approx \frac{1}{R_{\mathrm{g}} + R_{\mathrm{c}} + (L_{\mathrm{g}} + L_{\mathrm{c}})s}$$

This neglects the small current flowing into the filter capacitors and the stiff grid inductance $L_{\mathrm{grid}} \ll L_{\mathrm{g}}$.

SVPWM Scheme

There are three NPC legs (phases u, v, and w) shown in Fig. 2. Each leg contains four switches Qx1, Qx2, Qx3, and Qx4 (x = u, v, and w), and these four switches must be controlled in two complementary pairs. Qx1 and Qx3 make one complementary pair, while Qx2 and Qx4 make the other pair. By controlling these four switches the inverter output allows for three different voltage levels. Table 2 lists the three valid states for each leg, in which P means a switch leg is connected to the positive DC rail,

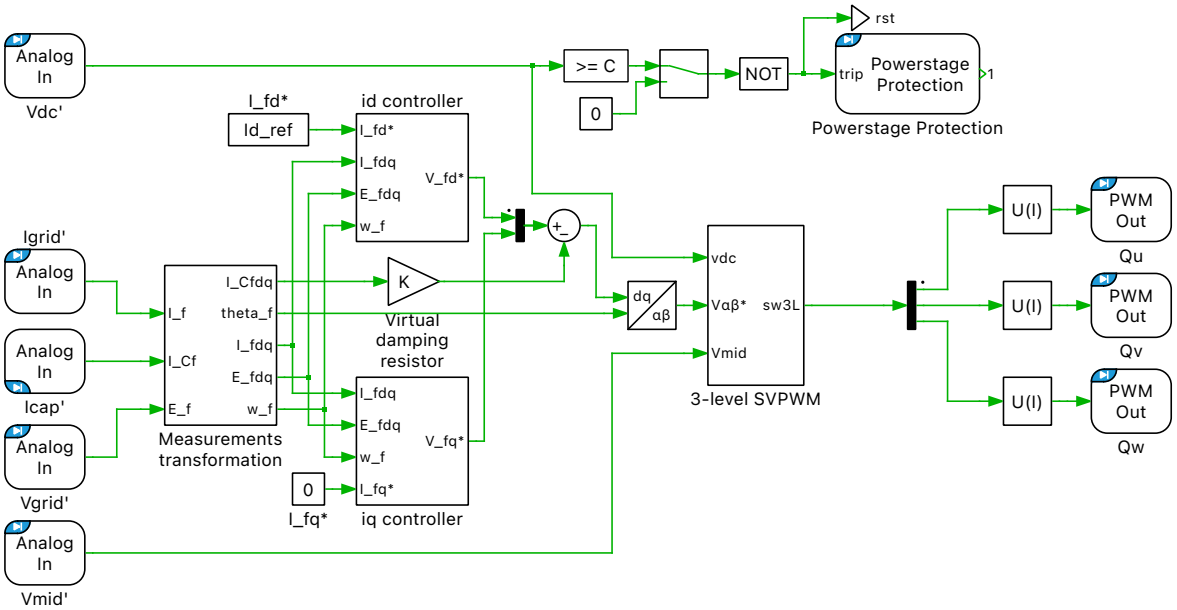


Figure 6: Control scheme of the grid-connected three-level NPC inverter using SVPWM method

N means it is connected to the negative DC rail, and O means it is connected to the neutral-point potential.

Table 2: Output status of each leg based on different switching combination of Qx1-Qx4

Switch No.	Qx1	Qx2	Qx3	Qx4	Phase voltage	Leg status
1	ON	ON	OFF	OFF	$\frac{V_{\mathrm{dc}}}{2}$	P
2	OFF	OFF	ON	ON	$-\frac{V_{\mathrm{dc}}}{2}$	N
3	OFF	ON	ON	OFF	0	O

Thus, in total there are 27 states of the three-level VSI which can be mapped to the space-vector diagram, depicted in Fig. 7. Assuming a reference vector V_{ref}, according to the theory of SVPWM, we need to find the two nearest vectors V_{X}, V_{Y} and one zero vector V_{Z} in order to synthesize V_{ref}. Therefore, vector PNN (V_{X}), PON (V_{Y}) and NNN (V_{Z}) in Fig. 7 can be selected accordingly to form V_{ref}.

If the dwelling time of vector V_{X}, V_{Y} and V_{Z} inside a switching period T_{sw} are T_{X}, T_{Y} and T_{Z} respectively, the following functions must be satisfied:

$$V_{\mathrm{X}}T_{\mathrm{X}} + V_{\mathrm{Y}}T_{\mathrm{Y}} + V_{\mathrm{Z}}T_{\mathrm{Z}} = V_{\mathrm{ref}}T_{\mathrm{sw}} \tag{1}$$

$$T_{\mathrm{X}} + T_{\mathrm{Y}} + T_{\mathrm{Z}} = T_{\mathrm{sw}} \tag{2}$$

However, it is difficult to determine V_{X}, V_{Y} and V_{Z} by the angle only, which is used in the 2-level SVPWM scheme, because the reference vector can be located in different sectors even if the angle is the same. To determine the sector, the amplitude of the reference vector is also needed, but this increases the complexity of the calculation.

Thus, [3] presented a simplified way to determine V_{X}, V_{Y} and V_{Z}, using the core of 2-level SVPWM. First, the whole vector diagram shown in Fig. 7 is divided into six main sectors. Each main sector has a shape of a sub-hexagon, and all six sub-hexagons distribute continuously with a 60° angle difference. Fig. 8 depicts sub-hexagon 1 and 2 as an example.

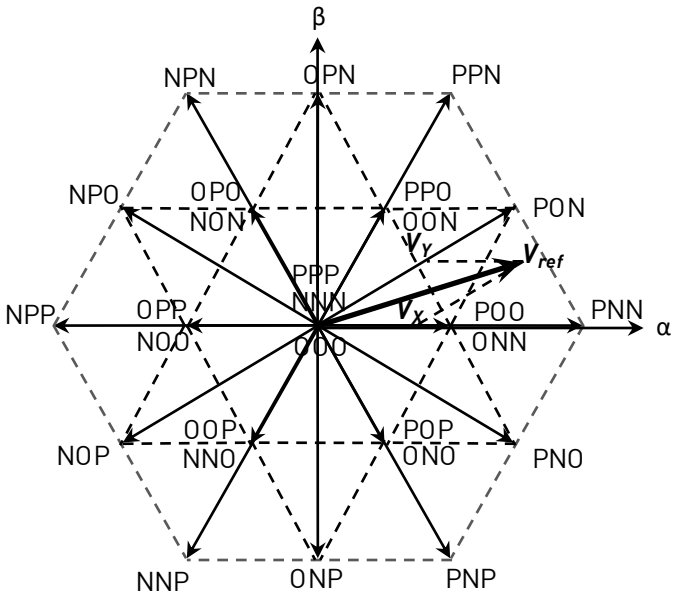


Figure 7: Three-phase three-level inverter SVPWM vector diagram

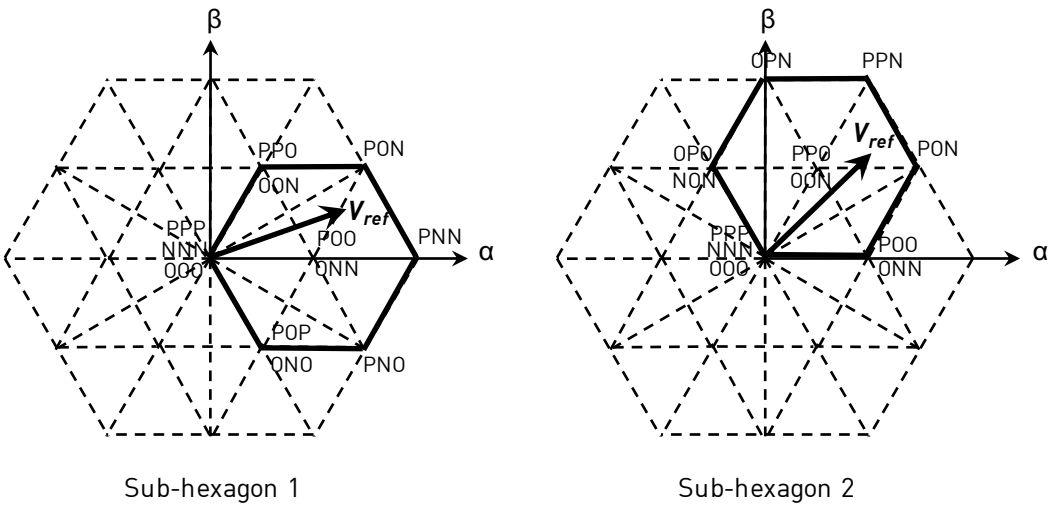


Figure 8: Sub-hexagon 1 and 2 out of the divided six sub-hexagons in the whole vector diagram

After the main sector (sub-hexagon) is determined, the original vectors must be mapped into the selected main sector. The mapping algorithm follows:

$$V' = V_{\text{original}} - V_{\text{map}} \tag{3}$$

For example the original vectors in the main sector 1 are PPP (OOO, NNN), POP (ONO), PNO, PNN, PON, PPO (OON), and POO (ONN). To get a hexagon similar to the 2-level SVPWM, take POO (ONN) as the mapping vector $V_{\text{map1}} = V_0$. After the mapping we can get the hexagon shown in Fig. 9, which is the same vector diagram as the 2-level SVPWM.

From Fig. 9, it can be seen that V'_{ref} is still in the mapped sub-hexagon 1, and we can easily determine that the dwelling vectors are V'_1 and V'_2. The V'_0 can be taken as the zero vector in the 2-level SVPWM. So, we can get the following function:

$$V'_1 T_{\text{X}} + V'_2 T_{\text{Y}} + V'_0 T_{\text{Z}} = V'_{\text{ref}} T_{\text{sw}} \tag{4}$$

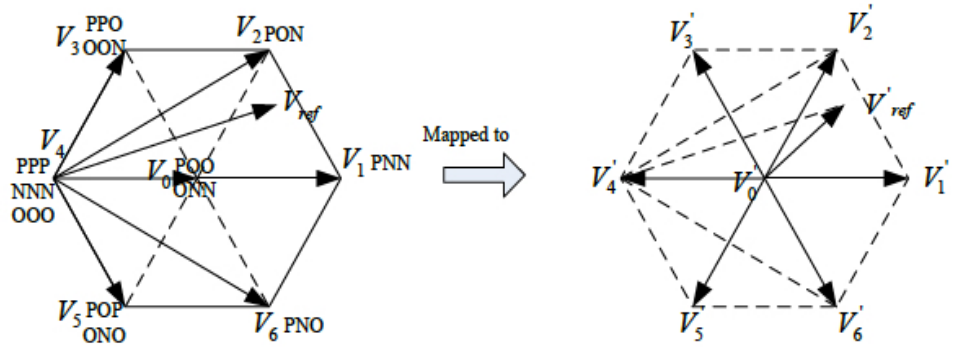


Figure 9: Mapping from the 3-level SVPWM to a 2-level SVPWM in sub-hexagon 1

Note that Eq. (2) is still valid here. Combing Eq. (2) and Eq. (4), one can derive:

$$(V_1 - V_{\text{map1}})T_{\text{X}} + (V_2 - V_{\text{map1}})T_{\text{Y}} + (V_0 - V_{\text{map1}})T_{\text{Z}} = (V_{\text{ref}} - V_{\text{map1}})T_{\text{sw}} \tag{5}$$

which means:

$$V_1 T_{\text{X}} + V_2 T_{\text{Y}} + V_0 T_{\text{Z}} = V_{\text{ref}} T_{\text{sw}} \tag{6}$$

Thus, if the dwelling time of V_1', V_2', and V_0' can be calculated, the original vector dwelling time can be determined. From the mapping in Fig. 9, the vector selection and the dwelling time calculation of the 3-level SVPWM are converted to 2-level SVPWM totally.

Different main sectors have different mapping vectors. Table 3 summarizes the mapping vector for each main sector.

Table 3: Mapping vector for each main sector

Main sector No.	Mapping vector	Element of α	Element of β
1	POO or ONN	$\frac{V_{\text{dc}}}{3}$	0
2	PPO or OON	$\frac{V_{\text{dc}}}{6}$	$\frac{\sqrt{3}V_{\text{dc}}}{6}$
3	OPO or NON	$-\frac{V_{\text{dc}}}{6}$	$\frac{\sqrt{3}V_{\text{dc}}}{6}$
4	OPP or NOO	$-\frac{V_{\text{dc}}}{3}$	0
5	OOP or NNO	$-\frac{V_{\text{dc}}}{6}$	$-\frac{\sqrt{3}V_{\text{dc}}}{6}$
6	POP or ONO	$\frac{V_{\text{dc}}}{6}$	$-\frac{\sqrt{3}V_{\text{dc}}}{6}$

The main sector number can be defined by the angle of the V_{ref} in the α-β coordinate plane. For example, according to Fig. 8, the angle range of main sector 1 is $[-\frac{\pi}{3}, \frac{\pi}{3}]$, and the angle range of main sector 2 is $[0, \frac{2\pi}{3}]$. Thus, the overlapped area between main sector 1 and 2 can be split into the two adjacent areas equally, in order to have monopolized angle area for each sector. Fig. 10 depicts the simplified definition of the six main sectors.

In the 2-level SVPWM, the first step is to find the sector number which can determine the dwelling vectors. The second step is to calculate the dwelling time for each of the selected vectors. According to the principle of 3-level SVPWM, when the main sector is determined and all the vectors are mapped to the main sector, the same process done in 2-level SVPWM can be implemented to determine the sub-sector and calculate the dwelling times for each dwelling vectors. Here in this demo model, a simple and effective way is deployed [3] to calculate the duty cycle for each switching pair out of the dwelling time of each dwelling vector.

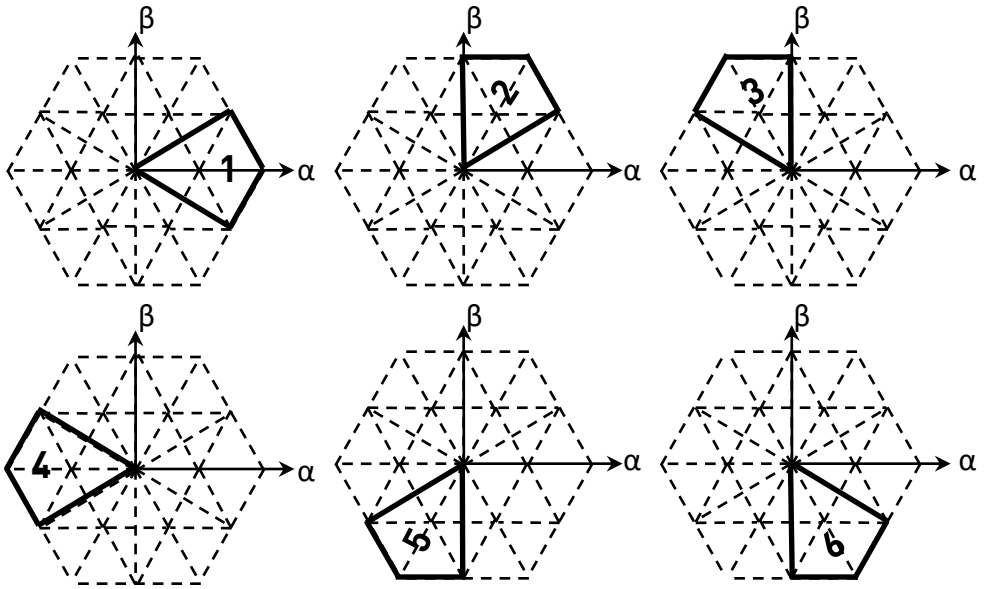


Figure 10: Simplified definition of the six main sectors

Again we take main sector 1 as an example. According to Fig. 8 there is no N status for u phase. Besides, if OON, ONO, and OOO are selected for the vector mapping, there will be no P status for the v and w phases. For the u phase, we represent the P status with 1, and the O status with 0. For v and w phases, we represent the O status with 1, and the N status with 0. Fig. 11 depicts this replacement operation. After this downsizing operation, the dwelling time for three vectors can be determined. As shown in Fig. 11, T_X is the dwelling time of status 100, T_Y represents the one of status 110, and T_Z is the time for status 111 and 000.

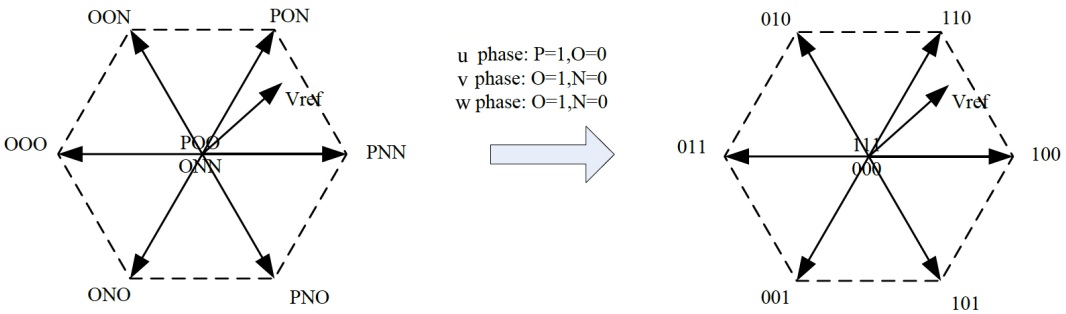


Figure 11: The status replacement rule downsizing 3-level vector diagram to 2-level one in main sector 1

Here we can calculate the three duty cycles for the upper switches out of the three complementary switch pairs (d1, d2, and d3), with the symmetrical PWM mode. The left side of Fig. 12 shows that effectively, the resulting 2-level vector sequence is 000 - 100 - 110 - 111- 110 - 100 - 000. Next, if we apply the same status replacement rule as in Fig. 11, we get the right part of Fig. 12. Thus we can achieve the 3-level vector sequence: ONN - PNN - PON - POO - PON - PNN - ONN.

Table 4 summarizes this status replacement rule for each main sector. The positive pair of power switches is Qx1 and Qx3 (x = u, v, w); the negative pair of the power switches is Qx2 and Qx4 (x = u, v, w). We also define the same status 0 and 1 for each pair as the 2-level SVPWM. So for the main sector 1, since in one switching cycle, u phase has no N status, the negative pair u phase is always 0. Similarly for the v and w phases, since they have no P status, the positive pair is always 0. That means in the main sector 1, d1 can be assigned to the positive pair of u phase (i.e. Qu1 has duty cycle of d1, and

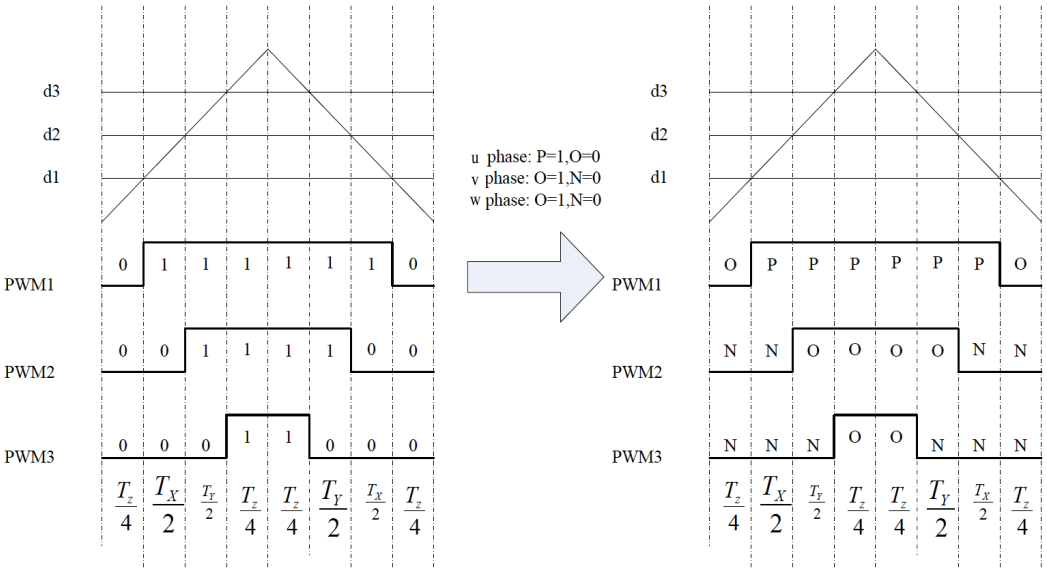


Figure 12: Symmetrical 2-level SVPWM applying the status replacement rule back to a 3-level SVPWM

Qu3 has complementary logic to Qu1), d2 can be assigned to the negative pair of v phase (i.e. Qv2 has duty cycle of d2, and Qv4 has complementary logic to Qv2), and d3 can be assigned to the negative pair of w phase (i.e. Qw2 has duty cycle of d3, and Qw4 has complementary logic to Qw2). The process can be extended to all the six main sectors and Table 5 shows this duty cycle assignment rule.

Table 4: Status replacement rule for each main sector

Main sector	U phase		V phase		W phase	
No.	1	0	1	0	1	0
1	P	O	O	N	O	N
2	P	O	P	O	O	N
3	O	N	P	O	O	N
4	O	N	P	O	P	O
5	O	N	O	N	P	O
6	P	O	O	N	P	O

The simplified 3-level SVPWM algorithm discussed above is implemented using the C-Script block and the output provides six modulation index values for Qu1, Qu2, Qv1, Qv2, Qw1 and Qw2 individually, as summarized in Table 5. The complementary signal for each of them is realized by configuring the opposite Polarity in the corresponding PWM Out blocks.

Neutral-point balancing technique

The active neutral-point balancing technique implemented in this demo model is based on [4]. Neutral-point current i_{NP} is denoted as the current coming out of the DC neutral point shown in Fig. 2. According to the SVPWM vector diagram shown in Fig. 7, Table 6 summarizes all the vectors that influence the neutral-point balance. $i_{\mathrm{u,v,w}}$ denotes the current direction going out of the switching node of the three-level phase leg entering the grid side.

Small vectors come in pairs, e.g. POO and ONN, and they disturb the neutral point with exactly the same current value, but just the opposite sign. Furthermore, as shown in Fig. 11, POO and ONN are the

Table 5: Duty cycle assignment rule for each main sector

Main sector No.	U phase		V phase		W phase	
	Positive pair (Qu1)	Negative pair (Qu2)	Positive pair (Qv1)	Negative pair (Qv2)	Positive pair (Qw1)	Negative pair (Qw2)
1	d1	1	0	d2	0	d3
2	d1	1	d2	1	0	d3
3	0	d1	d2	1	0	d3
4	0	d1	d2	1	d3	1
5	0	d1	0	d2	d3	1
6	d1	1	0	d2	d3	1

new zero vectors in the downsized 2-level vector diagram in main sector 1. Therefore, the active control of neutral-point voltage lies in the manipulation of this new zero vector pair. This requires measuring the middle-point voltage (v_{mid} in Fig. 2) in addition to the full DC voltage (v_{dc} in Fig. 2). As a result, the total zero vector dwelling time T_{Z} in Fig. 12 will be split between its 2-level "111" and "000" vectors, each proportional to its half DC voltage. Since the medium vectors disturb the neutral point and there is no vector that can be used to balance with the medium vector inside each main sector, some neutral-point variation can still be observed on the scale of each main sector. For more details and limitations of this method, please refer to [4].

Table 6: Neutral-point current i_{NP} for different space vectors

Positive Small Vectors	i_{NP}	Negative Small Vectors	i_{NP}	Medium Vectors	i_{NP}
ONN	i_{u}	POO	-i_{u}	PON	i_{v}
PPO	i_{w}	OON	-i_{w}	OPN	i_{u}
NON	i_{v}	OPO	-i_{v}	NPO	i_{w}
OPP	i_{u}	NOO	-i_{u}	NOP	i_{v}
NNO	i_{w}	OOP	-i_{w}	ONP	i_{u}
POP	i_{v}	ONO	-i_{v}	PNO	i_{w}

3 Simulation

This model can run both, in offline mode on a computer or in real-time mode on the PLECS RT Box. For the real-time operation, one RT Box (referred to as "Plant + Controller") needs to be set up as demonstrated in Fig. 13.

Note To utilize FPGA simulation on an RT Box 2 or 3, the Electrical Model Settings block connected to the power converter topology has to be configured as **Target: FPGA**. Please see the model initialization commands of this demo for more details.

Please follow the instructions below to run a real-time model on a single RT Box:

1 Connect the Analog Out interface to the Analog In interface with one DB37 cable, and the Digital Out interface to the Digital In interface with another DB37 cable (as shown in Fig. 13).

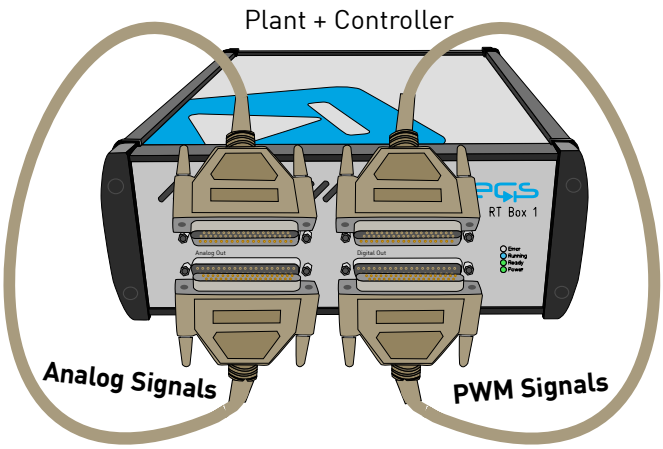


Figure 13: Hardware configuration for the real-time operation on a single RT Box

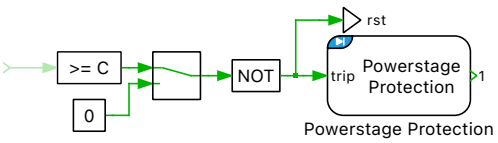
2 From the **System** tab of the **Coder options...** window, select the "Plant + Controller" subsystem and **Build** it onto the RT Box.

3 Once the model is uploaded, from the **External Mode** tab of the **Coder options...** window, **Connect** to the RT Box and **Activate autotriggering**.

Note As shown below, the Manual Signal Switch in the "Controller" task in its default "up" position enables switching, once the model is up and running.

Under external mode, changing it to the "down" position trips all PWMs into the safe state, and resets the id-iq PI Controller integral part to its initial condition.

The PWM safe state is configured in the Protection tab of each PWM Out block.



Key waveforms can be observed in the "Measurements" Scopes individually placed in the plant topology and the "Controller" task. Since the neutral-point balancing technique is implemented in the controller, the middle-point DC voltage can be controlled at around $400\,\mathrm{V}$ operating at steady state even though the initial voltages on the upper and lower DC capacitors are $450\,\mathrm{V}$ and $350\,\mathrm{V}$, respectively. A DC voltage step change can be applied on the "Sun" Constant block, such as from 1 to 1.2. This implies a sun radiation change on the PV panels. Fig. 14 captures the response to such an event on the inverter side. One can see that the middle-point DC voltage rises from $400\,\mathrm{V}$ to $480\,\mathrm{V}$, and stabilizes afterwards. Accordingly, grid currents are controlled to deliver the same d-q axis currents after short dynamics.

Next, keeping the DC voltage at the default value of $800\,\mathrm{V}$, on the controller side of the "Virtual damping resistor", the Gain block can be changed to 85 % of the original value ($(L_\mathrm{c} + L_\mathrm{g})/L_\mathrm{g} * R_\mathrm{D}$). A moderate amount of ringing in current waveforms can be observed due to inadequate damping. This is demonstrated in Fig. 15. Changing the "Virtual damping resistor" gain back to the original value, this unwanted ringing can be eliminated.

In the end, since PI controllers are designed individually for d-q axis currents, a d-axis current reference step-down is performed by changing the "I_fd^*" Constant block, such as to 80 % of its original value. Fig. 16 captures this reference step. The grid currents are controlled to the new d-axis reference value, while maintaining a power factor of 1 due to the unchanged q-axis current reference of 0.

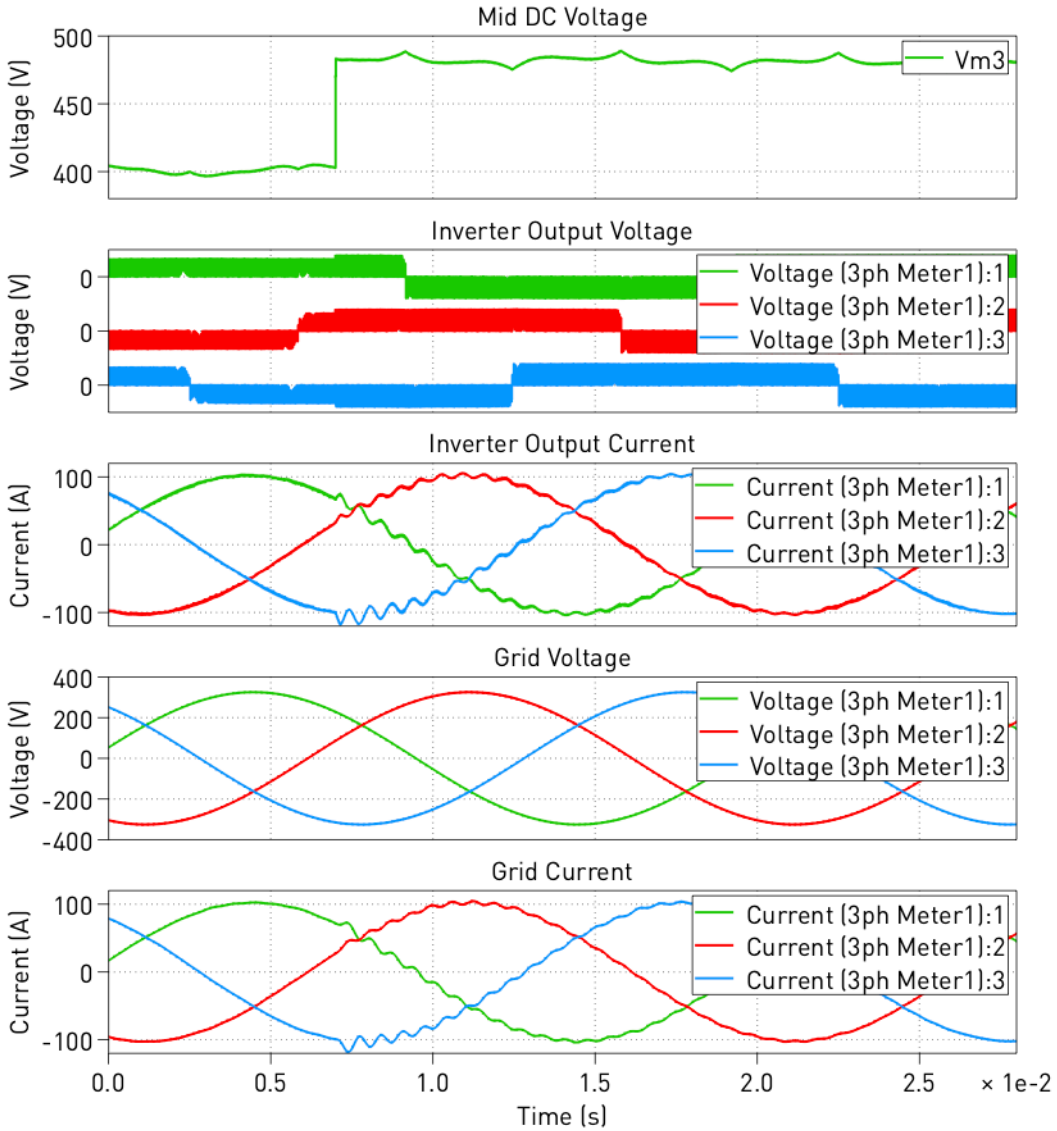


Figure 14: Real-time simulation result for inverter under DC voltage rise

4 Conclusion

This RT Box demo model demonstrates a three-level grid-connected NPC inverter under closed-loop control with d-q axis continuous PI current controllers. The demo model can run in both offline simulation and real-time operation for hardware-in-the-loop tests or rapid control prototyping. The plant model runs with a discretization step size of $5\ \mu s$ on the RT Box. The controller task runs with a discretization step size of $50\ \mu s$, which is the size of the switching period.

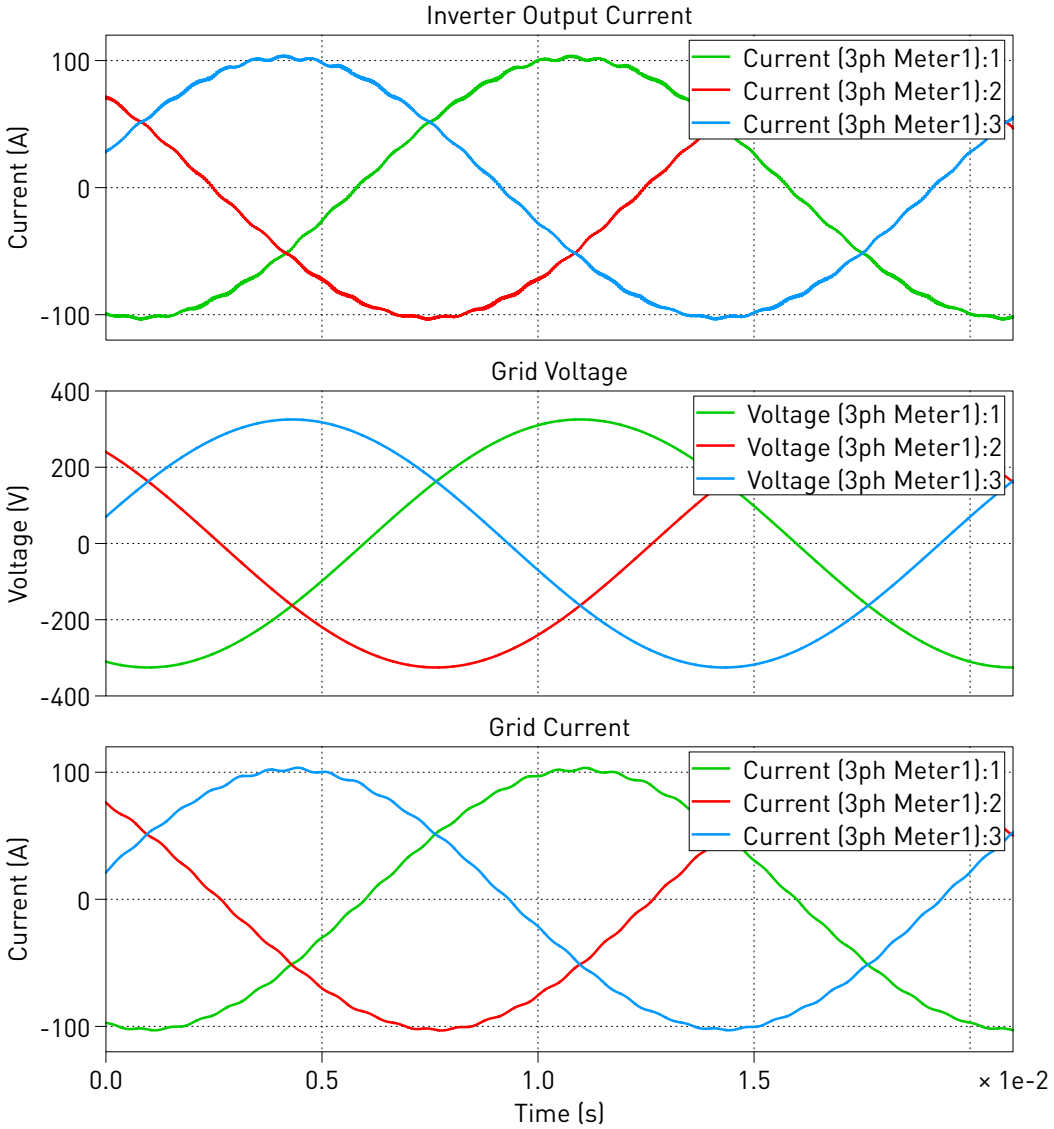


Figure 15: Real-time simulation result for inverter with poorly damped virtual resistor

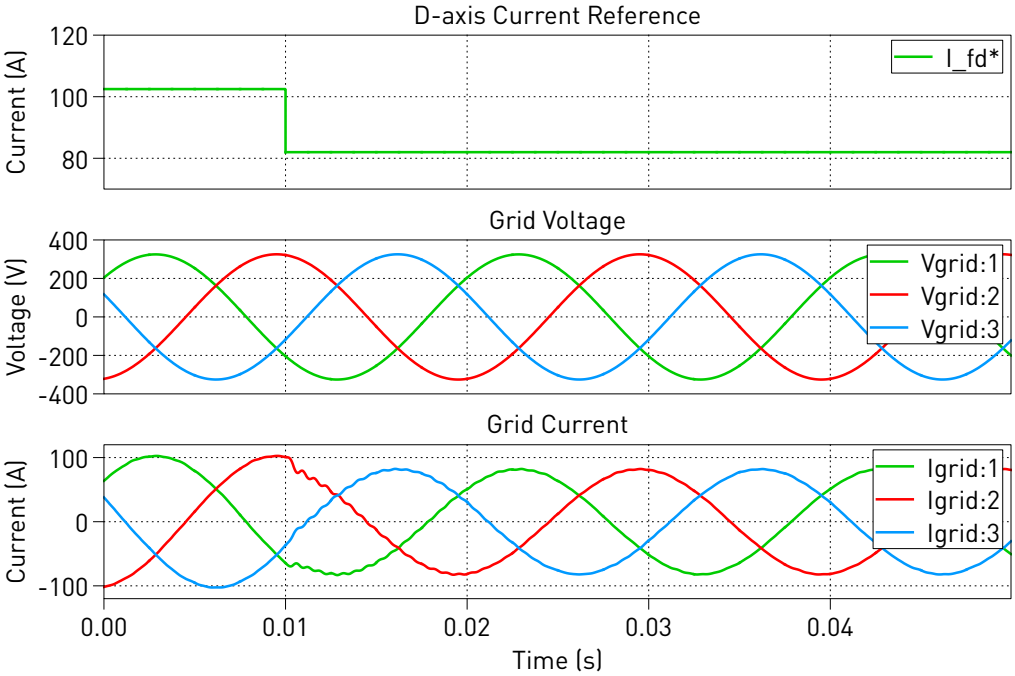


Figure 16: Controller task side real-time simulation result for inverter under d-axis current reference step

References

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[3] V. Xue, "Center-Aligned SVPWM Realization for 3-Phase 3-Level Inverter (Application Report)", Texas Instruments, October 2012.

[4] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters", *IEEE Transactions on Power Electronics*, vol. 15, no. 2, pp. 242-249, March 2000.

Revision History:

RT Box TSP 1.8.3	First release
RT Box TSP 2.1.7	Add the enable/disable switching scheme and use the PI Controller component from the library
RT Box TSP 2.2.1	Use the Powerstage Protection block to enable/disable switching
RT Box TSP 3.0.1	Update the single box model to use the multi-tasking feature on RT Box 1, and showcase FPGA simulation on RT Box 2 and 3
RT Box TSP 3.0.3	Remove the model with two separate RT Boxes and keep only the single RT Box model using multi-tasking feature

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RT Box Demo Model