

RT Box

DEMO MODEL

Fourth-Order Converters

Simulating Ćuk, SEPIC and Zeta converters using the Chopper Power Modules on the RT Box

Last updated in RT Box Target Support Package 4.1.1

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1 Overview

The Ćuk, SEPIC (Single-Ended Primary Inductor Converter), and Zeta converters are a family of fairly interesting converters that were introduced in the 1980s. They have been classified as fourth-order converters for the reason that each of these converters comprises four independent storage elements involving two inductors and two capacitors.

This demo showcases all three converters running in real-time on the RT Box, featuring:

- The converter topologies are built with Chopper (High-Side Switch) or Chopper (Low-Side Switch) component under PLECS library Power Modules, in their default `Sub-cycle average` configuration.
- The PWM signal generation uses a simple open-loop pattern on the same RT Box where the converter topology runs in real-time.
- To deploy the model on a single RT Box, a loopback cable is needed to connect together the Digital Out interface and the Digital In interface at the front panel of the Box.
- Due to the rather high switching frequencies of these converters, the FlexArray solver is more suitable than a CPU solver. Therefore only RT Box 2, 3 or 4 are intended for this demo. Furthermore, the existing Nanostep converters in PLECS Library cannot be applied to simulate these topologies. Therefore the Nanostep solver cannot be utilized here.

The chosen discretization step size for CPU and the FlexArray step size of each converter demo are shown in Tab. 1.

Table 1: Discretization step sizes of the fourth-order converter demos

Model Name	RT Box 2/3/4 CPU, FlexArray
Ćuk Converter	$1.5\,\mu$s, 125 ns
SEPIC Converter	$1.5\,\mu$s, 125 ns
Zeta Converter	$1.5\,\mu$s, 125 ns

1.1 Requirements

- One PLECS RT Box 2, 3 or 4[1] and one PLECS Coder[2] license.
- The RT Box Target Support Package[3] (minimum version 4.1.1).
- Follow the step-by-step instructions on configuring PLECS and the RT Box in the Quick Start guide of the RT Box User Manual[4].

2 Model

The original topologies of the three converters are depicted in Fig. 1. At steady state, the input-output voltage relationship is expressed in the following equation:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{d}{1-d}$$

where d indicates the duty cycle of the main switch S (MOSFET or IGBT).

The Ćuk, SEPIC, and Zeta converter design parameters (i.e., the values of L1, L2, C1, and C2) are taken from the Table 4, Table 5, and Table 6 in [1]. All three circuits operate under the same conditions:

[1] https://www.plexim.com/products/rt_box
[2] https://www.plexim.com/products/plecs/plecs_coder
[3] https://plexim.com/download/rt_box
[4] https://www.plexim.com/sites/default/files/rtboxmanual.pdf

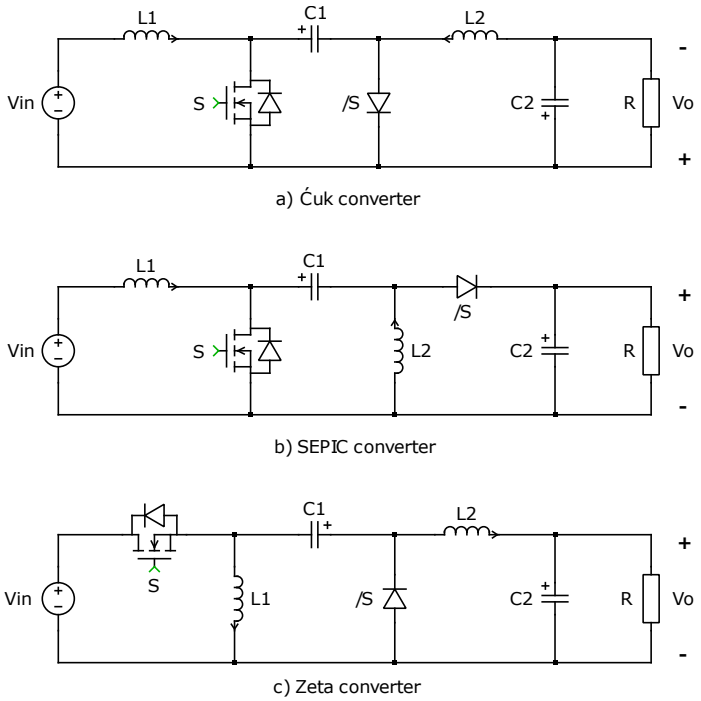


Fig. 1: Original circuit topologies for the Ćuk, SEPIC and Zeta converters

switching frequency $f_{\mathrm{sw}} = 100\,\mathrm{kHz}$; input voltage $V_{\mathrm{in}} = 100\,\mathrm{V}$; load resistor $R = 100\,\Omega$. The converters operate in open loop with a fixed duty cycle of $d = 2/3$ to facilitate the comparison.

2.1 Basic Switching Cells

A canonical switching cell was introduced in [2]. It contains two passive elements (one capacitor and one inductor) and two switches operated complementary, as shown in Fig. 2 (a). The Ćuk converter is derived from this basic switching cell [3]. A second basic switching cell, introduced in [3] and hereafter referred to as the "singular switching cell", contains the same number of passive and switching components arranged differently, as shown in Fig. 2 (b).

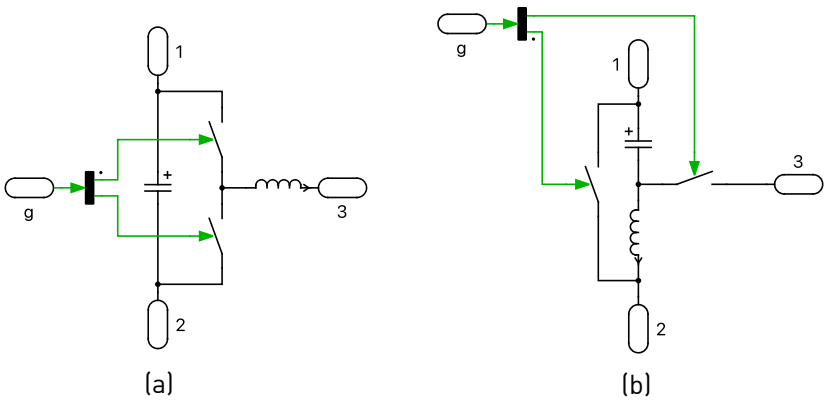


Fig. 2: The basic switching cell (a) and the singular switching cell (b) based on a capacitor, an inductor, and two switching devices

2.2 Implementation of the Switching Cells Based on the Half-Bridge Hybrid Model

Canonical switching cell

The canonical switching cell already has the port behavior expected by the half-bridge hybrid model: voltage-source behavior between terminal 1 and 2 and a current-source behavior at terminal 3. If terminal 3 is connected to an external inductor, as in the case of the Ćuk converter, the internal inductor can be set to zero. This enables a direct implementation of the canonical switching cell without requiring further circuit manipulations. By connecting the source and load to the switching cell, Ćuk converter can be constructed, as shown in Fig. 3.

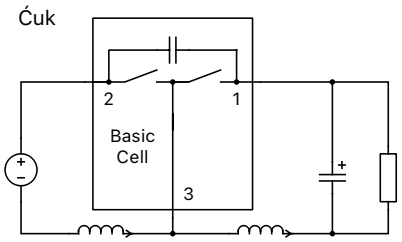


Fig. 3: Ćuk converter based on the basic switching cell

Singular switching cell

The derivation of the singular switching cell based on the hybrid half-bridge model requires a few circuit manipulations, as shown in Fig. 4.

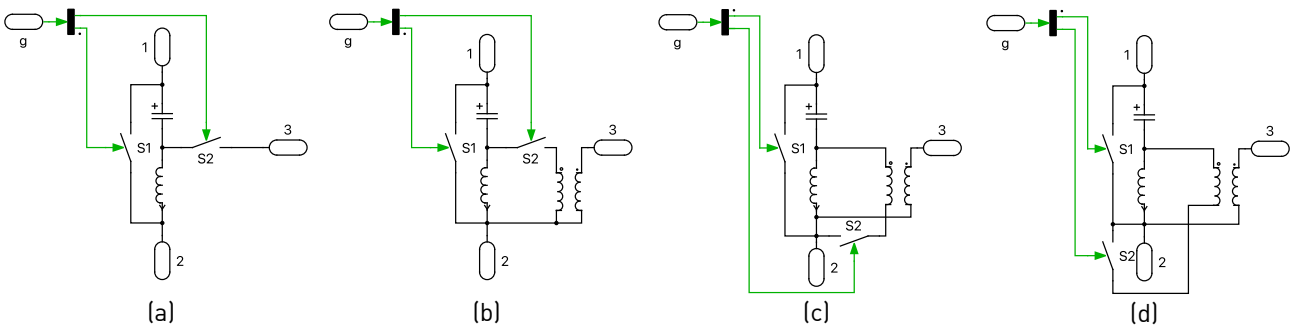


Fig. 4: Derivation of the singular switching cell based on the half-bridge hybrid converter model in four steps (a) to (d)

1 A voltage-source type of load/source is assumed between terminals 2 and 3.

2 An ideal transformer with a $1 : 1$ ratio is inserted between terminals 2 and 3. This transformer is redundant, and does not alter the current or voltage waveforms.

3 Switch S2 is moved along its current path through the transformer.

4 Switch S2 is rotated 90 degrees clockwise, placing the two switches in series and making the half-bridge arrangement visible.

The two switches S1 and S2 of the circuit in Fig. 4 can now be replaced by a half-bridge hybrid model. By connecting different types of source and load, or by adding additional passive elements, the SEPIC and Zeta converters can be constructed with the singular switching cell [3], as shown in Fig. 5. It clearly shows why Zeta converter is considered the “inverse SEPIC” converter.

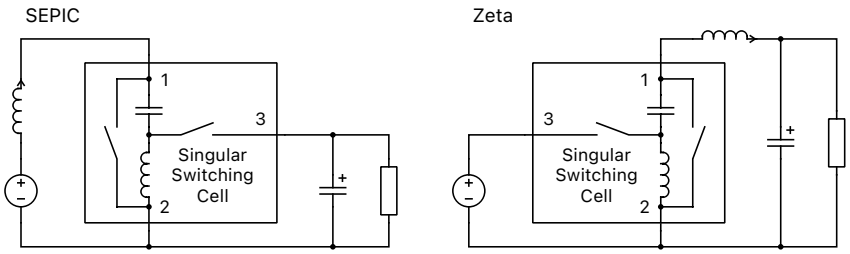


Fig. 5: SEPIC and Zeta converter based on the singular switching cell

3 Simulation

These models can run both in offline mode on a computer or in real-time mode on the PLECS RT Box. For the real-time operation, one RT Box 2, 3 or 4 needs to be set up as demonstrated in Fig. 6.

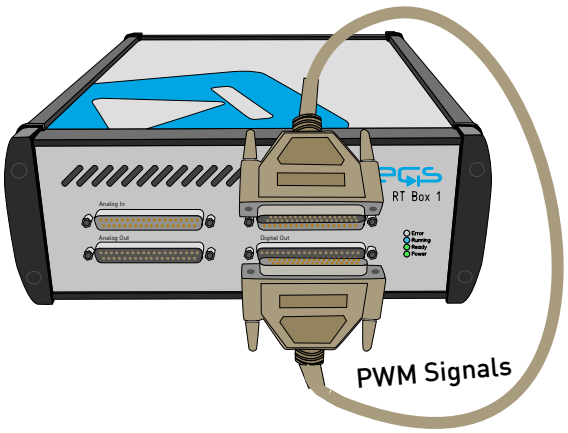


Fig. 6: Single RT Box with a loopback cable connected in front to run the demos

1. From the **System** tab of the **Coder options…** window, select the "Plant" and **Build** it onto the user's RT Box.
2. Once the model is uploaded, from the **External Mode** tab of the **Coder options…** window, **Connect** to the RT Box and **Activate autotriggering**.
3. The user can view the real-time waveforms from the Scopes connected inside the "Plant" subsystem schematic.
4. The user can also find more CPU or FPGA simulation real-time performance information under the **Application** and **Diagnostics** tabs of the RT Box Web Interface.

Fig. 7 compares the results of the original ideal-switching Ćuk, SEPIC, and Zeta converter simulated offline in PLECS using a variable-step solver, with those of their individually derived equivalent circuits running in real-time on a PLECS RT Box 2 using the FPGA-based FlexArray solver at the step size of 125 ns. This comparison demonstrates the validity of the circuit derivation discussed previously in Section "Implementation of the Switching Cells Based on the Half-Bridge Hybrid Model".

4 Conclusion

Switching cells provide a structured approach to generating DC–DC converter topologies. For each switching cell, the input and load can be altered to form new converter topologies. Implementing specific switching cells based on sub-cycle averaging enables high-fidelity real-time simulation models for

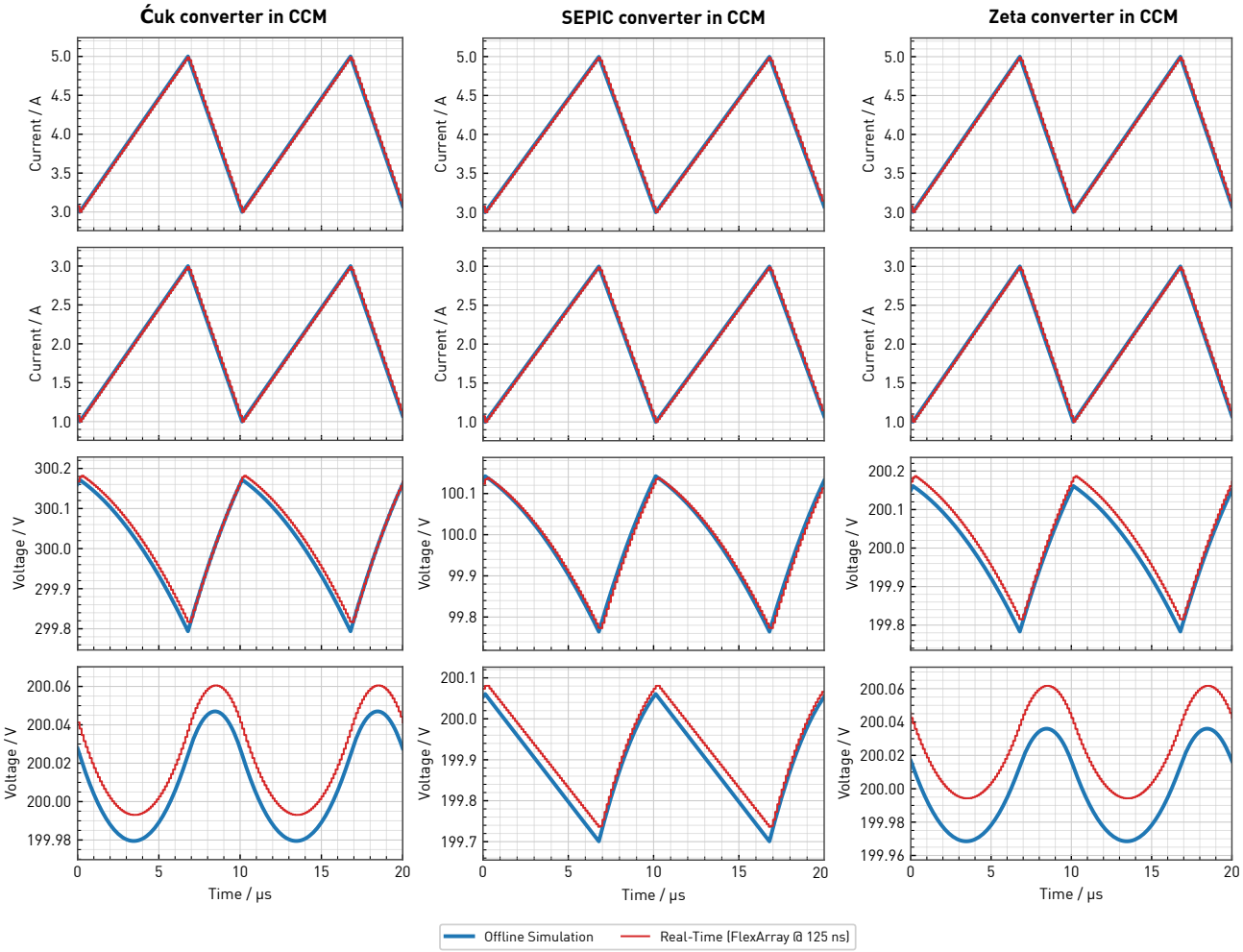


Fig. 7: Offline vs. real-time simulation result of the Ćuk, SEPIC and Zeta converters at $f_{\mathrm{sw}} = 100\,\mathrm{kHz}$

the derived converter topologies. This enhances the reusability of existing real-time simulation modeling building blocks. Two basic switching cells are used in this demo to demonstrate the concept. From these two switching cells, Ćuk, SEPIC and Zeta converter topologies can be derived. The comparison between PLECS offline simulation results obtained using a variable-step solver, and real-time simulation on the PLECS RT Box using the FPGA-based FlexArray solver shows good agreement.

5 Bibliography

[1] **1** Garza-Arias, J. C. Rosas-Caro, J. E. Valdez-Resendiz, J. C. Mayo-Maldonado, G. Escobar-Valderrama, D. Guillen, and A. Rodríguez, "The Fourth-Order Single-Switch Improved Super-Boost Converter with Reduced Input Current Ripple", Electronics, vol. 10, no. 19, 2021.

[2] **1** Landsman, "A unifying derivation of switching dc-dc converter topologies", in IEEE Power Electronics Specialists Conference (PESC), 1979, pp. 239–243.

[3] **1** Bauwelz Gonzatti, Y. Li, M. Amirabadi, B. Lehman, and F. Z. Peng, "An overview of converter topologies and their derivations and interrelationships," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 10, no. 6, pp. 6417–6429, 2022.

Revision History:

RT Box TSP 4.1.1	First release

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