

RT Box

DEMO MODEL

Minimal Example Demos

Last updated in RT Box Target Support Package 4.1.1

www.plexim.com

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- Get the latest RT Box Target Support Package
- Check the PLECS and RT Box TSP documentation

1 Overview

These RT Box minimal example demos feature basic power converter topologies running on a single RT Box. These demo models have the following features:

- The converter topologies are built with components under PLECS library Nanostep modules, if applicable, or with PLECS library Power Modules in their default `Sub-cycle average` configuration.
- The PWM signal generation uses a simple open-loop pattern, on the same RT Box where the converter topology runs in real-time.
- To deploy the model on a single RT Box, a loopback cable is needed to connect together the Digital Out interface and the Digital In interface at the front panel of the Box.

This document describes a common concept of the minimal example demos. It focuses on showcasing the execution capability of the RT Box for basic converter topologies. Please note that here is no intention of providing actual parameters for a real-world converter design.

The chosen discretization step size and average execution time for CPU, the FlexArray and Nanostep (when applicable) step size of each minimal example demo are shown in Tab. 1. The RT Box's Nanostep solver simulates the converter with time steps in the single-digit nanosecond range. The step size of the Nanostep solver is fixed based upon the RT Box hardware, which is 7.5 nanoseconds on the RT Box 1 and CE and 4 nanoseconds on the RT Box 2, 3 and 4. The small step size is critical to accurately model high-frequency DC/DC converters with an inductive AC link.

Table 1: Discretization step sizes of the minimal example demos

Model Name	RT Box 1 CPU	RT Box 2/3/4 CPU, FlexArray	Nanostep (7.5 ns on RT Box 1, 4 ns on RT Box 2/3/4)
Buck Converter	1.25 μs	1.25 μs , 54 ns	Yes
Synchronous Buck Converter	1.25 μs	1.25 μs , 54 ns	Yes
Boost Converter	1.25 μs	1.5 μs , 54 ns	Yes
Boost PFC Converter	1.25 μs	1.5 μs , 54 ns	Yes
Boost PFC Converter with LC Filter	1.25 μs	1.5 μs , 54 ns	Yes
Flyback converter	1.5 μs	1.5 μs , 94 ns	Yes
Single-Phase Inverter	1.5 μs	1.5 μs , 54 ns	Yes
Single-Phase Inverter with LCL Filter	1.5 μs	1.5 μs , 54 ns	Yes
Three-Phase Four-Leg Inverter	2.0 μs	2.0 μs , 74 ns	Yes
Three-Phase Inverter	2.0 μs	2.0 μs , 54 ns	Yes
Three-Level NPC Inverter	2.0 μs	2.0 μs , 61 ns	Yes
Three-Level NPC Inverter (two interleaved branches with breakers)	5.0 μs	2.0 μs , 182 ns	N/A
Three-Level T-Type Inverter	2.0 μs	2.0 μs , 61 ns	Yes
Three-Level ANPC Inverter	2.5 μs	2.0 μs , 154 ns	N/A
Five-Level ANPC Inverter	3.0 μs	2.5 μs , 192 ns	N/A
Vienna Rectifier	2.0 μs	2.0 μs , 74 ns	Yes
Five-Phase Inverter	5.0 μs	2.5 μs , 139 ns	N/A

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Table 1 – continued from previous page

Model Name	RT Box 1 CPU	RT Box 2/3/4 CPU, FlexArray	Nanostep (7.5 ns on RT Box 1, 4 ns on RT Box 2/3/4)
Five-Phase Interleaved Sync. Buck	3.5 μs	2.5 μs , 139 ns	N/A
Flying-Cap Single-Phase Inverter	5.0 μs	2.5 μs , 179 ns	N/A
Cascaded Full-Bridge Rectifier	5.0 μs	1.8 μs , 600 ns	N/A
Dual-Active Bridge	1.8 μs	1.8 μs , 55 ns	Yes
Half-Bridge LLC	1.8 μs	1.8 μs , 55 ns	Yes
Full-Bridge LLC	1.8 μs	1.8 μs , 55 ns	Yes
Phase-Shifted Full-Bridge	1.8 μs	1.8 μs , 55 ns	Yes
Bidirectional Phase-Shifted Full-Bridge	1.8 μs	1.8 μs , 60 ns	Yes
CLLLC	2.0 μs	2.0 μs , 54 ns	Yes
NPC CLLLC	2.0 μs	2.0 μs , 61 ns	Yes
Three-Phase Dual Active Bridge	2.0 μs	2.0 μs , 54 ns	Yes
Triple Active Bridge	2.0 μs	2.0 μs , 61 ns	Yes

1.1 Requirements

To run these demos, the following items are needed (available at www.plexim.com[1]):

- PLECS[2] and PLECS Coder[3] license, min. version 5.0.7 required
- One PLECS RT Box (CE, 1, 2, 3 or 4)[4]
- The RT Box Target Support Package[5], min. version 4.1.1 required
- Follow the step-by-step instructions on configuring PLECS and the RT Box in the Quick Start guide of the RT Box User Manual[6].
- One 37 pin Sub-D cable

Note

This model contains model initialization commands that are accessible from:
PLECS Standalone: the menu **Simulation > Simulation Parameters... > Initializations**
PLECS Blockset: right click in the **Simulink model window > Model Properties > Callbacks > InitFcn***

2 Model

Since all the minimal example demos follow the same self-loopback concept, below we use the Flying-Capacitor Single-Phase Inverter model for illustration. Fig. 1 depicts the top-level schematic of the mini-

[1] https://www.plexim.com
[2] https://www.plexim.com/products/plecs/plecs_standalone
[3] https://www.plexim.com/products/plecs/plecs_coder
[4] https://www.plexim.com/products/rt_box
[5] https://www.plexim.com/download/rt_box
[6] https://www.plexim.com/sites/default/files/rtboxmanual.pdf

mal example model.

The users can add a Scope at the top-level schematic to visualize the generated ideal PWM signals in an offline simulation on the PC.

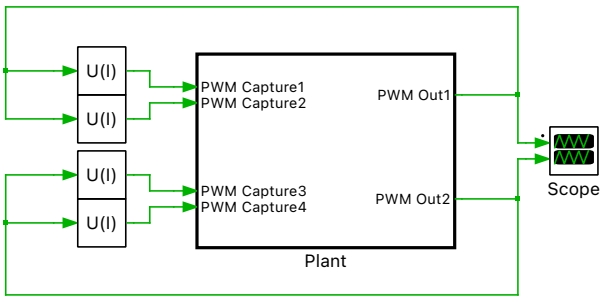


Fig. 1: Top-level schematic of a minimal example demo

The “Plant” Subsystem includes both the converter topology and the PWM generation logic. Fig. 2 shows the circuit model inside the “Plant” Subsystem.

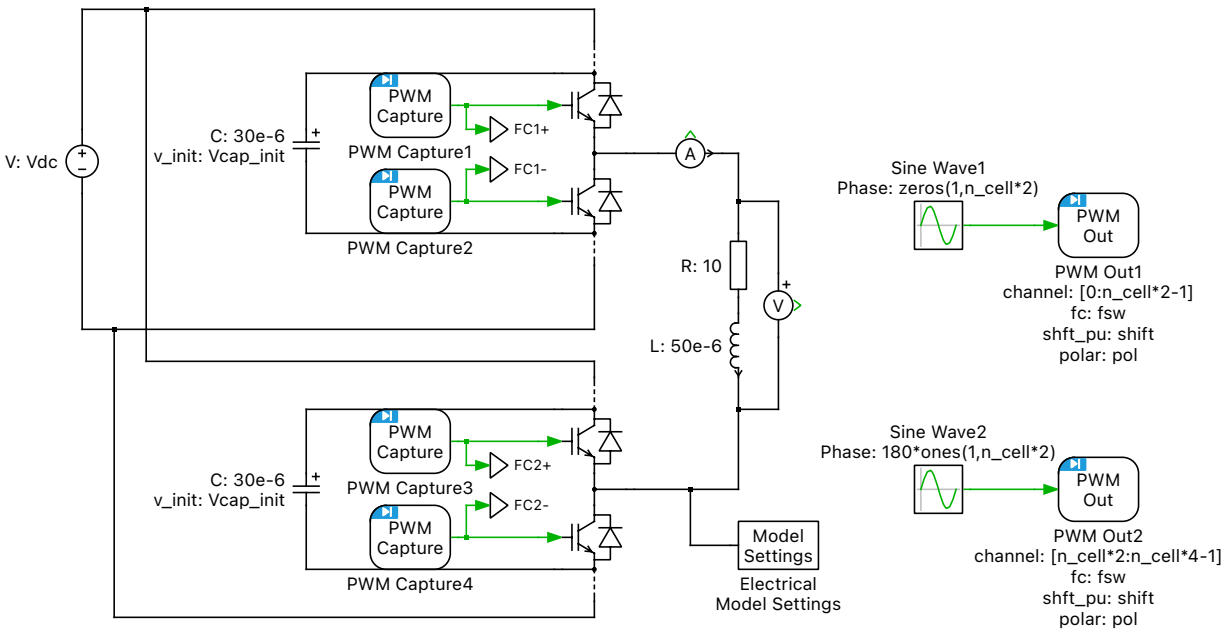


Fig. 2: Plant subsystem schematic of a minimal example demo

2.1 Converter topology

If applicable, the converter’s switching legs are build with modules available in the Nanostep section of the PLECS library. The RT Box’s Nanostep solver simulates the converter with time steps in the single-digit nanosecond range. If a topology does not have a Nanostep implementation, it is modeled using a Power Module from the PLECS library in the default `Sub-cycle average` configuration.

The `Assertions` inside the Power Modules are all configured as the default **On**. During real-time running, an overlapping in gating signals of the complementary switch pair can be caught. RT Box will throw an error message.

An Electrical Model Settings block is connected to the converter bridge leg. Inside this block, the **Target** can be chosen as **CPU** or **FlexArray**.

- CPU - available on all RT Boxes, also the default option for building onto an RT Box CE or 1.

- FlexArray - only available on RT Box 2, 3 and 4, therefore the default option for building onto an RT Box 2, 3 or 4.

Also, the discretization step size `Ts_plant` may be adjusted slightly between different simulation targets. Please see the model initialization commands of each demo for more details.

2.2 PWM generation and capturing

PWM Out blocks from the RT Box target support library are used to generate PWM signals. Configurations such as `Carrier phase shift`, `Carrier limits`, or `Polarity`, are utilized to generate gating signal patterns for different topologies in a versatile way on the RT Box.

PWM Capture blocks from the RT Box target support library are used to sample in the self-generated PWM signals in the loopback way. Note that for FPGA simulation, a prerequisite is that the PWM Capture blocks have to be connected directly to the gates of the Power Modules - this is already the case in all minimal example demo implementation. If the Power module is configured for Nanostep, the PWM signaled are sampled with an interval of 7.5 nanoseconds on the RT Box 1 and CE and 4 nanoseconds on the RT Box 2, 3 and 4, which is the Nanostep solver execution interval.

3 Simulation

Please follow the instructions below to deploy a minimal example model onto a single RT Box:

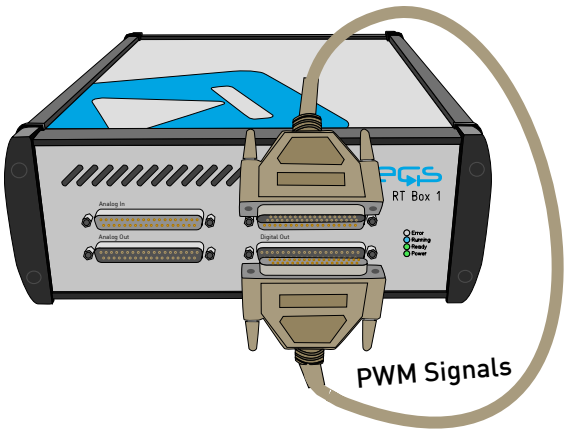


Fig. 3: Single RT Box with a loopback cable connected in front to run the minimal example demos

1. Connect the Digital Out interface to the Digital In interface of a single RT Box, using a DB37 cable shown in Fig. 3.
2. From the **System** tab of the **Coder options...** window, select the "Plant" and **Build** it onto the user's RT Box.
3. Once the model is uploaded, from the **External Mode** tab of the **Coder options...** window, **Connect** to the RT Box and **Activate autotriggering**.
4. The user can view the real-time waveforms from the Scopes connected inside the "Plant" subsystem schematic.
5. The user can also find more CPU or FPGA simulation real-time performance information under the **Application** and **Diagnostics** tabs of the RT Box Web Interface.

4 Conclusion

These minimal example demos showcase the simple usage of a single RT Box in PWM signal loopback setup. CPU or FlexArray simulation can be configured in the PLECS model with the corresponding set-

ting of the Electrical Model Settings block.

Revision History:

RT Box TSP 3.0.1	First Release
RT Box TSP 3.0.3	Add the NPC inverter demo with two interleaved branches
RT Box TSP 3.1.2	Update demos to Nanostep solver, add various new topologies
RT Box TSP 3.2.2	Update demos to feature the Nanostep Scope, add the Boost PFC converter demo
RT Box TSP 4.0.2	Add three-phase four-leg demo
RT Box TSP 4.1.1	Add two demos of Boost PFC Converter with LC Filter and Single-Phase Inverter with LCL Filter

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RT Box Demo Model

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