

RT Box

DEMO MODEL

Datacenter Power Distribution System

A 1 MW hybrid MVAC-LVDC transformer with active filter

Last updated in RT Box TSP 4.1.1

www.plexim.com

- Request a PLECS and PLECS Coder trial license
- Get the latest RT Box Target Support Package
- Check the PLECS and RT Box TSP documentation

1 Overview

This RT Box demo model features a hybrid medium-voltage AC (MVAC) to low-voltage DC (LVDC) transformer for datacenters, as shown in Fig. 1, as proposed by Huber et al. [1]. A 12-pulse diode rectifier supplies a $1\,\mathrm{MW}$ load at a DC bus voltage of $800\,\mathrm{V}$ ($\pm 400\,\mathrm{V}$) from a $13.2\,\mathrm{kV}$ grid through a low-frequency transformer (LFT) with a star and a delta secondary winding. An active filter (AF) with a rating of $300\,\mathrm{kVA}$ is connected to a third low-voltage winding of the same transformer. It compensates the current harmonics and the reactive power of the rectifier, so that the grid currents become sinusoidal at unity power factor. As in the auxiliary converter of Hou and Tsai [2], the AF has its own DC link, which is connected to the DC bus through a diode. The AF can therefore also return power to the grid when batteries or photovoltaic (PV) systems in the datacenter feed back into the DC bus. The AF is controlled in the rotating reference frame with PI and resonant current controllers and space-vector pulse-width modulation (PWM).

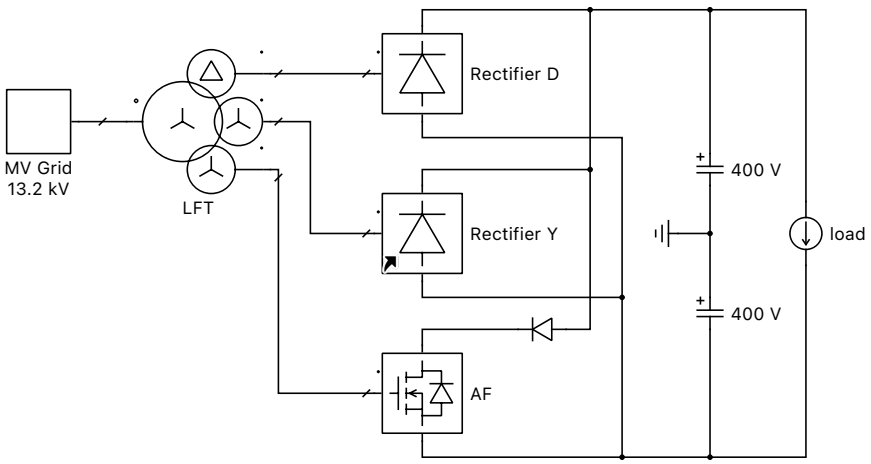


Fig. 1: System overview including MVAC grid, LFT, 12 pulse rectifier and the active filter

The model is set up for real-time simulation on a single RT Box 2, 3 or 4: the electrical circuit, including the diode rectifiers and the sub-cycle average model of the AF, runs on the FPGA-based FlexArray solver. One CPU core handles the plant-side signal processing, including the load profile, power analysis, and scopes, while a second CPU core runs the controller. The plant and controller exchange analog and digital signals through physical loop-back connections on the RT Box front panel. Tab. 1 lists the discretization step sizes.

Table 1: Discretization step sizes and average execution times on one RT Box 2, 3 or 4

Processing unit	Step size	Execution time
CPU core 0	$5\,\mu\mathrm{s}$ (`Ts_plant`)	$2.2\,\mu\mathrm{s}$
CPU core 1	$50\,\mu\mathrm{s}$ (`Ts_ctrl`)	$3.8\,\mu\mathrm{s}$
FlexArray solver	$625\,\mathrm{ns}$	–

1.1 Requirements

To run this demo model, the following items are needed (available at www.plexim.com[1]):

- One PLECS RT Box 2, 3 or 4[2]. The RT Box CE and the RT Box 1 do not provide the FlexArray solver.

[1] https://www.plexim.com
[2] https://www.plexim.com/products/rt_box

- One PLECS[3] and one PLECS Coder[4] license
- The RT Box Target Support Package[5]
- Follow the step-by-step instructions on configuring PLECS and the RT Box in the Quick Start guide of the RT Box User Manual[6].
- Two 37-pin D-Sub cables to loop back the analog and the digital signals on the front panel

Note

This model contains model initialization commands that are accessible from:
PLECS Standalone: the menu **Simulation > Simulation Parameters... > Initializations**
PLECS Blockset: right click in the **Simulink model window > Model Properties > Callbacks > InitFcn***

2 Model

The top-level schematic in Fig. 2 contains the subsystem "Plant + Controller", which is enabled for code generation (**Edit > Subsystem > Execution settings...**). Its target ports represent the I/Os of the RT Box. In the offline simulation, the wires at the top level emulate the loop-back cables, and the Delay blocks emulate the latency of one control period $T_\mathrm{s} = 1/f_\mathrm{sw} = 50\,\mu\mathrm{s}$ of the real-time controller.

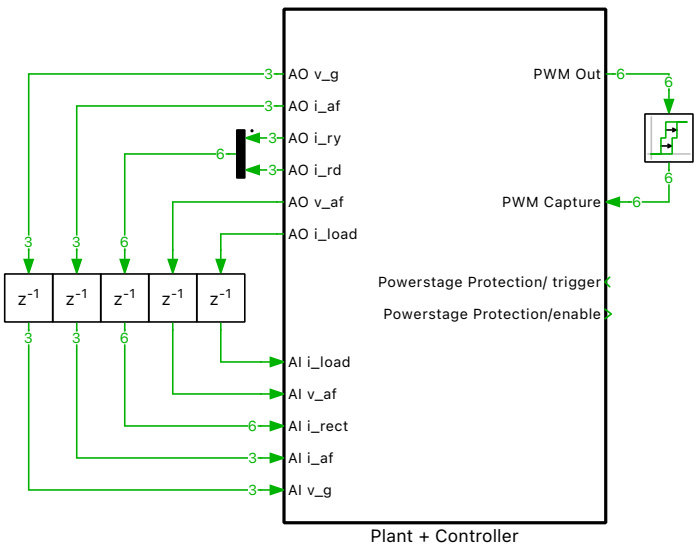


Fig. 2: Top-level schematic with the loop-back connections for the offline simulation

2.1 Plant + Controller

Fig. 3 and Fig. 4 on p. 6 show the content of the subsystem "Plant + Controller". It uses the multi-tasking mode (**Coder > Coder options... > Scheduling**) with the base task on CPU core 0 (step size `Ts_plant` = 5 μs) and the task "Control" on core 1 (step size `Ts_ctrl` = `1/fsw` = 50 μs). The yellow Task Frame "Control" assigns the Analog In blocks, the control algorithm and the PWM generation to the task "Control". The Scopes and plant-side signal processing logic run in the base task. The electrical system and the Analog Out blocks are updated with the FlexArray step size.

[3] https://www.plexim.com/products/plecs/plecs_standalone
[4] https://www.plexim.com/products/plecs/plecs_coder
[5] https://www.plexim.com/download/rt_box
[6] https://www.plexim.com/sites/default/files/rtboxmanual.pdf

The electrical circuit is calculated by the FlexArray solver. The FlexArray solver is only available on the RT Box 2, 3 and 4. The RT Box sets the FlexArray step size automatically to the smallest integer fraction of `Ts_plant` that is longer than the required calculation time and shows it on its display and in its web interface.

2.2 Plant

The plant's main parameters are listed in Tab. 2. The MV grid is modeled by a three-phase voltage source of $13.2\,\mathrm{kV}$ (line-to-line, rms) and $50\,\mathrm{Hz}$ and the grid impedance for a short-circuit power of $100\,\mathrm{MVA}$ at $X/R = 10$ ($L_\mathrm{g} = 5.52\,\mathrm{mH}$, $R_\mathrm{g} = 0.173\,\Omega$).

Table 2: Main parameters of the power circuit

Parameter	Value
MV grid: voltage (line-to-line, rms), frequency	$13.2\,\mathrm{kV}$, $50\,\mathrm{Hz}$
MV grid: short-circuit power, X/R ratio	$100\,\mathrm{MVA}$, 10
LFT: rated power; rectifier windings; AF winding	$1\,\mathrm{MVA}$; $2 \times 500\,\mathrm{kVA}$, $605\,\mathrm{V}$; $300\,\mathrm{kVA}$, $400\,\mathrm{V}$
LFT: short-circuit reactance MV-rectifier, rectifier-rectifier, MV-AF	$4\,\%$, $6\,\%$, $4\,\%$
LFT: winding resistance, no-load current, core losses	$0.3\,\%$, $0.5\,\%$, $1.2\,\mathrm{kW}$
Rectifier diodes: forward voltage, on-resistance	$0.75\,\mathrm{V}$, $0.6\,\mathrm{m\Omega}$
DC bus capacitance	$2 \times 20\,\mathrm{mF}$ in series ($10\,\mathrm{mF}$)
AF: switching frequency, dead time	$20\,\mathrm{kHz}$, $0.2\,\mu\mathrm{s}$
AF: L_f, C_f, R_d, C_AF	$40\,\mu\mathrm{H}$, $50\,\mu\mathrm{F}$, $0.2\,\Omega$, $3\,\mathrm{mF}$
Regeneration diode: forward voltage, on-resistance; "L_dr", "R_dr"	$0.9\,\mathrm{V}$, $1\,\mathrm{m\Omega}$; $10\,\mu\mathrm{H}$, $5\,\mathrm{m\Omega}$

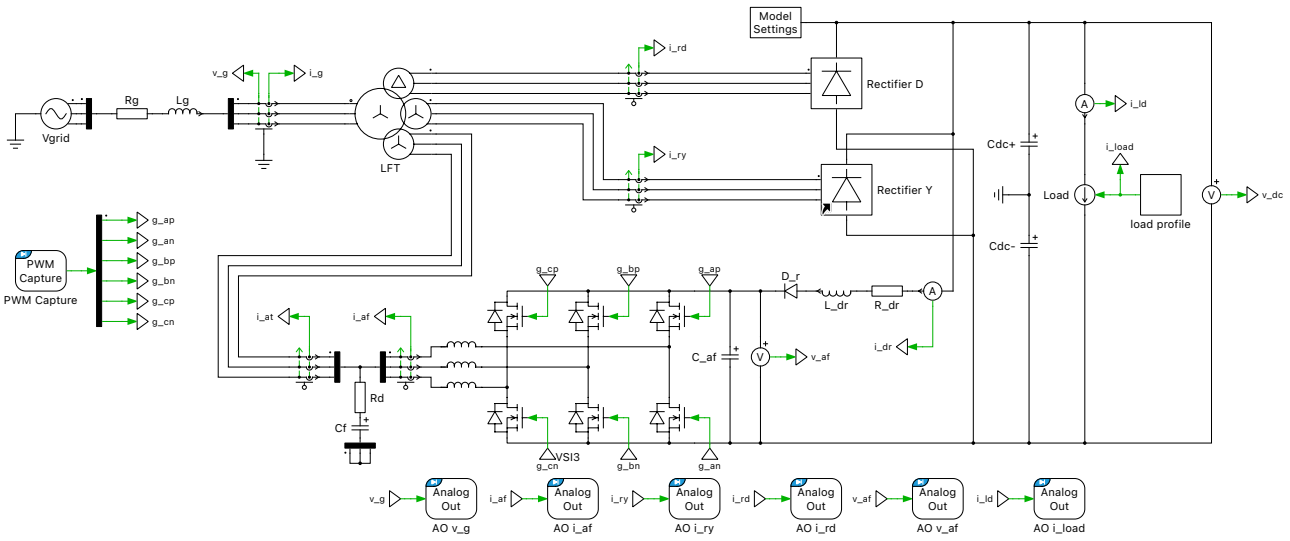


Fig. 3: Electrical system with MV grid, transformer, 12-pulse rectifier, DC bus and active filter

Low-frequency transformer

The $1\,\mathrm{MVA}$ LFT has four windings on one core: the MV winding in star connection, two $605\,\mathrm{V}$ rectifier windings of $500\,\mathrm{kVA}$ each in delta (Yd1) and star (Yy0) connection, and the $400\,\mathrm{V}$, $300\,\mathrm{kVA}$ AF winding in star connection (Yy0). The delta winding shifts the voltages of "Rectifier D" by 30° with respect to those of "Rectifier Y", so that the 5th and 7th harmonics of the two six-pulse rectifiers cancel in the MV current [1].

The LFT implements the star-equivalent circuit of the multi-winding transformer. The series impedance of the MV winding (R_p, L_p) and the magnetizing inductance L_m form the common branch. A Ydy Transformer block for the rectifier windings and a Yy Transformer block for the AF winding contain the leakage inductances and resistances of the low-voltage windings; their own magnetizing inductances are set to $1{,}000$ times L_m, so that their magnetizing currents are negligible. The core losses are represented by the core loss resistance of the Ydy Transformer block, and saturation is not modeled. The star-equivalent reactances follow from the short-circuit reactances $u_\mathrm{k} = 4\,\%$ between the MV winding and each rectifier winding and $u_\mathrm{ss} = 6\,\%$ between the two rectifier windings (both on $500\,\mathrm{kVA}$):

$$x_\mathrm{P} = u_\mathrm{k} - \frac{u_\mathrm{ss}}{2} = 1\,\%, \qquad x_\mathrm{S} = \frac{u_\mathrm{ss}}{2} = 3\,\% \tag{1}$$

This gives $L_\mathrm{p} = 11.1\,\mathrm{mH}$ on the MV side and $L_\mathrm{s} = 69.9\,\mu\mathrm{H}$ for the star winding; the delta winding uses $3L_\mathrm{s}$. Since the rectifiers are connected in parallel without an interphase transformer, the leakage inductance between the two rectifier windings must be large enough to prevent interbridge currents and the model uses $6\,\%$. The AF winding has a short-circuit reactance of $4\,\%$ with respect to the MV winding (on $300\,\mathrm{kVA}$).

12-pulse rectifier and DC bus

"Rectifier D" and "Rectifier Y" are Diode Rectifier blocks whose diodes model $1.6\,\mathrm{kV}/350\,\mathrm{A}$ dual-diode modules. Their DC sides are connected in parallel. The DC bus consists of two $20\,\mathrm{mF}$ capacitors with a grounded midpoint. The controlled current source "Load" represents the rack power supplies of the datacenter. A 1D Look-Up Table generates the load current from the simulation time using the profile shown in Fig. 6 of [1]. The current is initially $1{,}250\,\mathrm{A}$, corresponding to $1\,\mathrm{MW}$ at $800\,\mathrm{V}$. From $0.15\,\mathrm{s}$ to $0.21\,\mathrm{s}$, it ramps down to $-300\,\mathrm{A}$; the negative current represents power fed back from batteries or photovoltaic systems. The current remains constant until $0.25\,\mathrm{s}$ and then ramps back to $1{,}250\,\mathrm{A}$ by $0.315\,\mathrm{s}$. The profile repeats with the period `T_load`, which is set to $0.5\,\mathrm{s}$. The rectifier winding voltage is set to $605\,\mathrm{V}$ to produce a DC voltage of $800\,\mathrm{V}$ at half load.

Active filter

The power stage of the AF is a two-level voltage source inverter (VSI), modeled with the 3-Phase Voltage Source Inverter module in the sub-cycle average configuration. Its LCL filter consists of the converter-side inductor L_f, the star-connected filter capacitors C_f with the damping resistors R_d, and the grid-side inductance. The grid-side inductance comprises the leakage inductance of the AF winding together with the MV-side inductances. Referred to the AF winding, these inductances amount to $L_{\mathrm{g,AF}} = 73.0\,\mu\mathrm{H}$ (`Lg_af`). The AF has its own DC-link capacitor C_AF. The regeneration diode "D_r" connects the positive rail of the DC bus through the busbar or choke "L_dr", "R_dr" with the positive terminal of the AF DC link, and the negative rails are connected directly.

2.3 Controller

The controller contains a Three-Phase PLL and the control algorithm in Fig. 4, which is sampled once per PWM period, $T_\mathrm{s} = 50\,\mu\mathrm{s}$. The PLL (SRF-PLL with the basic controller design) estimates the phase angle θ and the amplitude $\hat{V}_\mathrm{g}$ of the MV phase voltages. With θ, the transformations into the rotating reference frame align the d-axis with the grid voltage estimated by the PLL, so that the d- and q-components of a current are its active and reactive components.

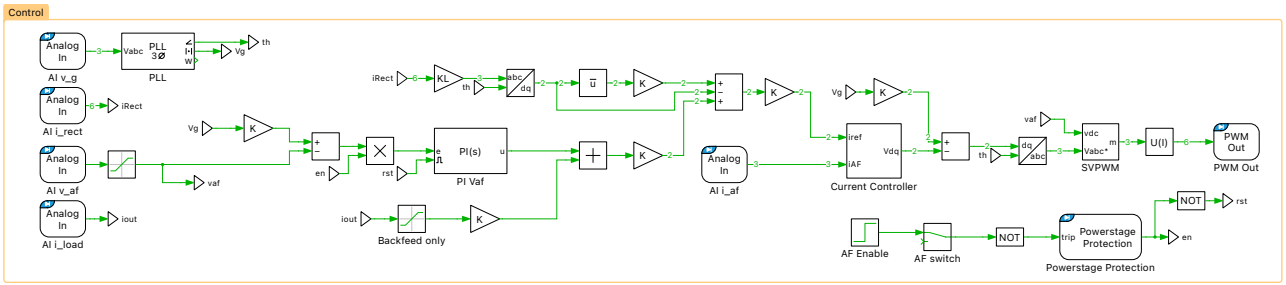


Fig. 4: Controller of the active filter

DC-link voltage control and reverse power flow

The reference of the AF DC-link voltage is

$$V_{\mathrm{AF}}^{*} = 1.02 \cdot \sqrt{3}\, k_{\mathrm{L}} \hat{V}_{\mathrm{g}} \tag{2}$$

i.e. $2\,\%$ above the peak line-to-line voltage of the rectifier windings, which is the no-load voltage of the rectifier ($V_{\mathrm{AF0}} = 872.7\,\mathrm{V}$ at nominal grid voltage). In rectifier operation, the DC bus voltage stays below this value, and the regeneration diode blocks. When the load feeds back, the rectifiers stop conducting, the DC bus voltage rises until the regeneration diode conducts, and the AF returns the power to the grid.

The voltage-controller output is limited to $\pm 18.6\,\mathrm{A}$ (`Ireg`), which corresponds to an active power of $300\,\mathrm{kW}$, the rating of the AF. The Gain "Regen FF" adds the feedforward term $V_{\mathrm{AF0}}/(1.5\,\hat{V}_{\mathrm{g}}) \cdot \min(I_{\mathrm{load}}, 0)$, which converts the measured backfeed power into a d-current.

Current control and modulation

The current controller acts on the error $\mathbf{e} = \mathbf{i}_{\mathrm{AF}}^{*} - \mathbf{i}_{\mathrm{AF}}$ of the AF converter currents in the rotating reference frame. It consists of the PI controller "PI i" and four resonant terms at 6, 12, 18 and 24 times the grid frequency, which correspond to the harmonic pairs 5/7, 11/13, 17/19 and 23/25 in the stationary frame. While the AF is disabled (`en` = 0), the errors of both PI controllers and of the resonant terms are zero, so that the integrators hold their values.

3 Simulation

3.1 Offline Simulation

The simulation runs from $t = -0.1\,\mathrm{s}$ to $0.35\,\mathrm{s}$ with the **auto** variable-step solver (maximum step size $1\,\mathrm{ms}$, relative tolerance 10^{-3}), so that the passive 12-pulse rectifier is in steady state at $t = 0$. The AF is enabled at $t = 50\,\mathrm{ms}$, and the load follows the profile described above. The values in Tab. 3 were measured in windows of one grid period. P, Q and the THD are the outputs of the subsystem "Grid Power Analyzer" (scope "Scope Grid Power") at the end of the window; the grid current and the power factor of phase a were calculated from the data of the scope "Scope AC and DC". The meter "PCC" measures the phase voltages and currents at the point of common coupling (PCC). In Fig. 3 on p. 4, the corresponding signals are labeled `v_g` and `i_g`, respectively.

Table 3: Measured values of the offline simulation

Quantity	AF off	AF on	Backfeed
Time window	$0.02 \ldots 0.04\,\mathrm{s}$	$0.12 \ldots 0.14\,\mathrm{s}$	$0.23 \ldots 0.25\,\mathrm{s}$

continues on next page

Table 3 – continued from previous page

Quantity	AF off	AF on	Backfeed
Load current I_{load}	1,250 A	1,250 A	−300 A
Active power P at the PCC	993 kW	1,005 kW	−244 kW
Reactive power Q at the PCC	270 kvar	3.0 kvar	1.8 kvar
Grid current, phase a (rms)	45.3 A	44.0 A	10.7 A
THD of the grid current	6.7 %	1.4 %	1.2 %
Power factor, phase a	0.963	0.9999	−0.9999
DC bus voltage V_{DC} (mean)	785.9 V	794.4 V	867.7 V
AF DC-link voltage V_{AF} (mean)	873.8 V	872.6 V	865.1 V

Fig. 5 shows the scope "Scope AC and DC". After the activation of the AF, the grid current becomes sinusoidal and in phase with the grid voltage. During the backfeed between 0.21 s and 0.25 s, the grid current is in phase opposition to the grid voltage, and the AF current referred to the MV side equals the grid current, since the rectifiers do not conduct. The DC bus voltage rises during the backfeed.

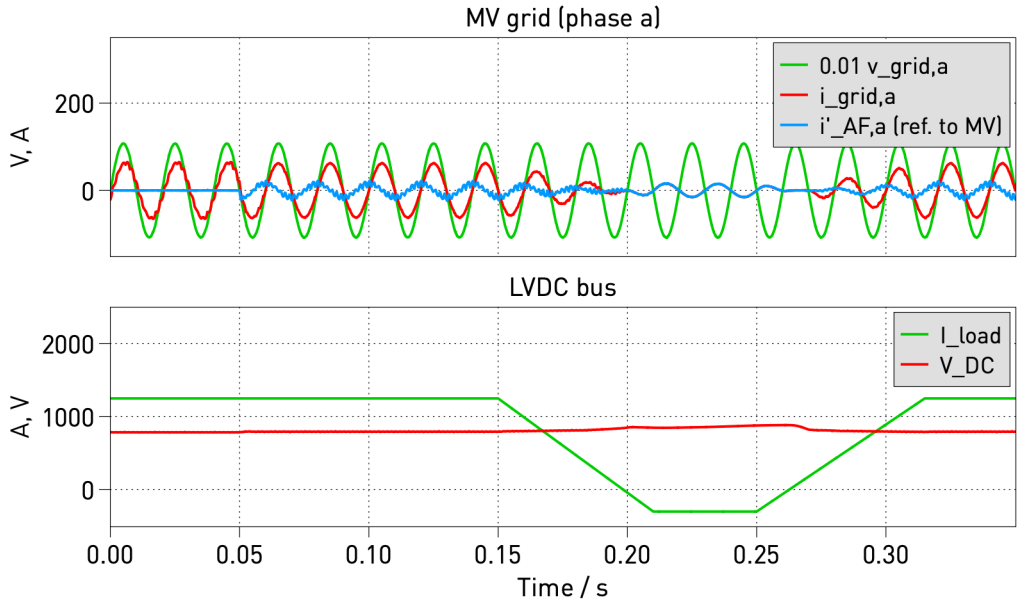


Fig. 5: MV grid voltage and currents of phase a, DC load current and DC bus voltage

Passive rectifier

Before 50 ms, the circuit operates as a passive 12-pulse rectifier. Fig. 6 shows the input currents of the rectifiers. Each rectifier draws the typical current of a six-pulse rectifier with a capacitive DC link, with two current peaks per half period, and the currents of "Rectifier D" are shifted by 30° with respect to those of "Rectifier Y". The activation of the AF hardly affects these currents. In the MV current, the 5th and 7th harmonics cancel, and the 11th (5.7 %) and the 13th harmonic (3.0 %) dominate (Fig. 7 on p. 9). The rectifier draws a reactive power of 270 kvar, i.e. 27 % of its active power, which corresponds to a power factor of $\lambda = 0.963$.

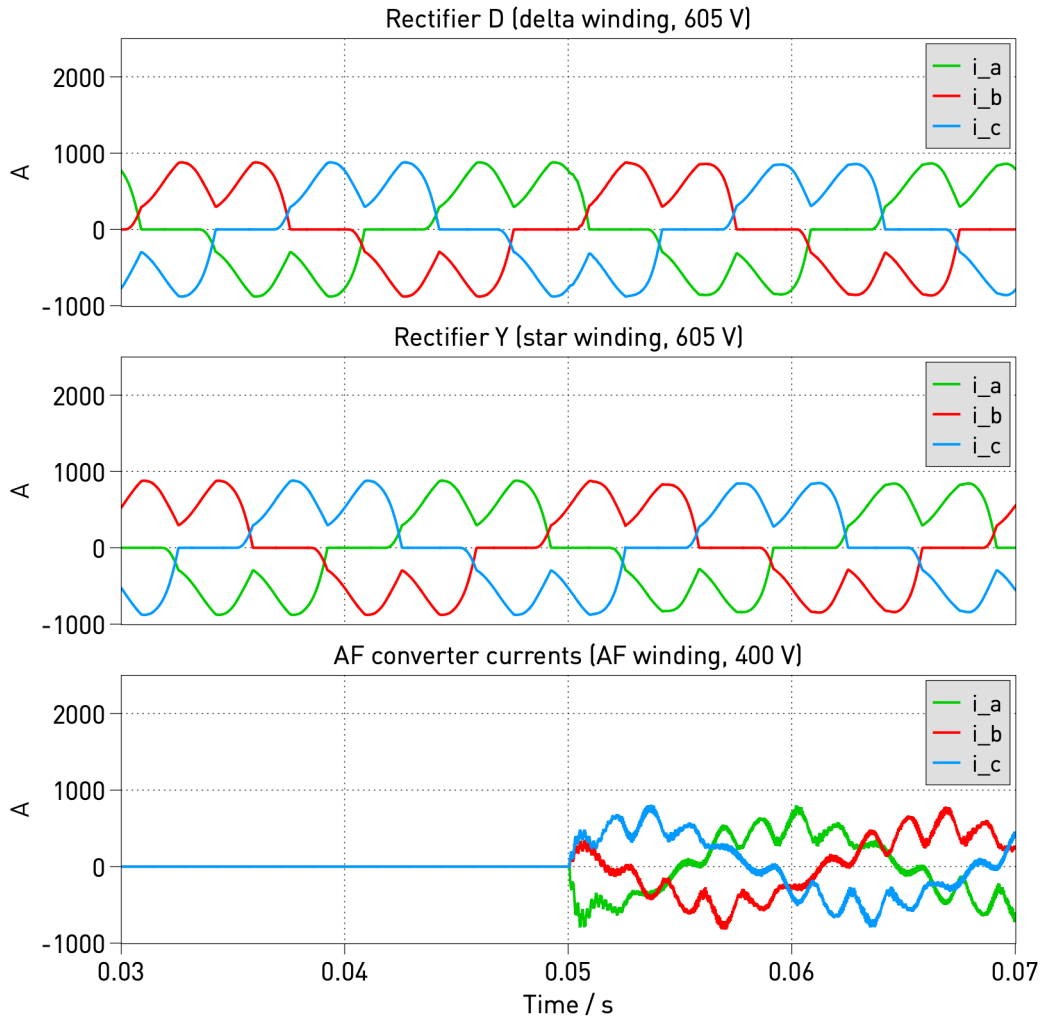


Fig. 6: Input currents of the two rectifiers and AF converter currents around the activation of the AF at 50 ms

Active filter operation

With the AF, the THD of the grid current drops from 6.7 % to 1.4 %, and the reactive power at the PCC from 270 kvar to 3 kvar (Fig. 8 on p. 10). The THD, calculated over the preceding grid period, stays below 2 %. The resonant terms reduce the 11th and 13th harmonics to 0.5 % and 0.6 % and the 23rd and 25th harmonics to 0.3 % (Fig. 7). The 35th and 37th harmonics (about 0.5 %) lie above the highest resonant frequency and are not reduced. The rms value of the AF converter current is 393 A, which corresponds to 272 kVA at the AF winding voltage of 400 V. The AF DC-link voltage oscillates at 600 Hz with an amplitude of 12 V, since the AF supplies the 11th and 13th harmonic currents, as can be seen the Scope "Scope DC Link" at simulation time 0.1 s.

The THD in Fig. 8 on p. 10 rises during the load reversal (off scale), since it refers to the fundamental of the grid current, which becomes small around zero power; the Function block "THD in %" limits it to 50 %.

Reverse power flow

Fig. 9 on p. 10 shows the DC side during the backfeed. When the load current becomes negative at 0.198 s, the rectifiers stop conducting and the load charges the DC bus capacitors. At 0.201 s, the DC bus voltage reaches the AF DC-link voltage, and the regeneration diode starts to conduct. The AF re-

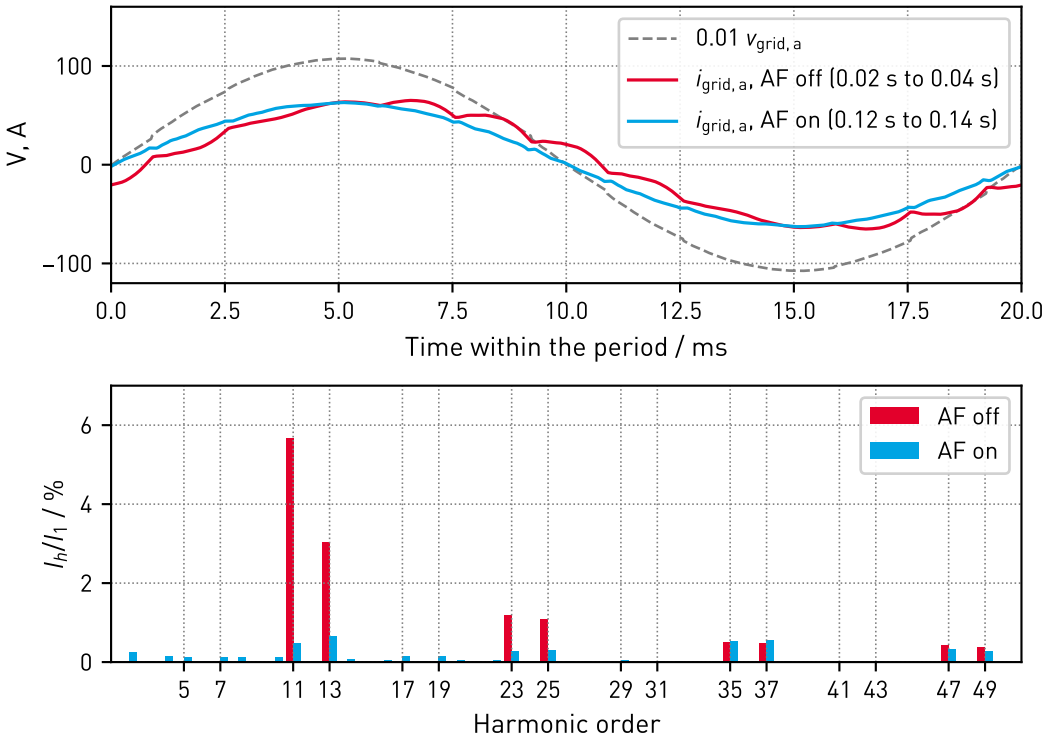


Fig. 7: Grid current of phase a over one period and its harmonics at full load, without and with active filter

turns the power to the grid with a power factor of -0.9999 and a THD of $1.2\,\%$. After the load current has become positive again, the diode blocks, and the DC bus voltage decreases until the rectifiers conduct again.

Without the AF, the backfeed cannot be returned to the grid due to the unidirectional nature of the diode rectifiers and the DC bus voltage starts to rise. To simulate this scenario, set the Manual Switch “AF Switch” to off.

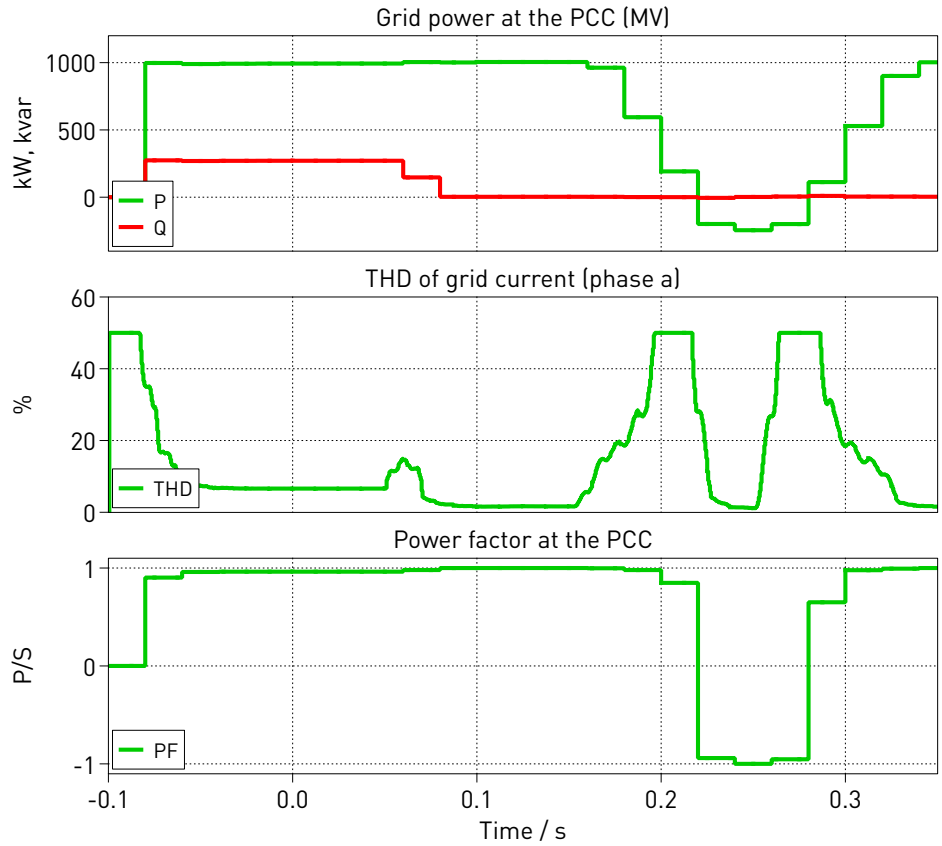


Fig. 8: Active and reactive power at the PCC and THD of the grid current, averaged over one grid period

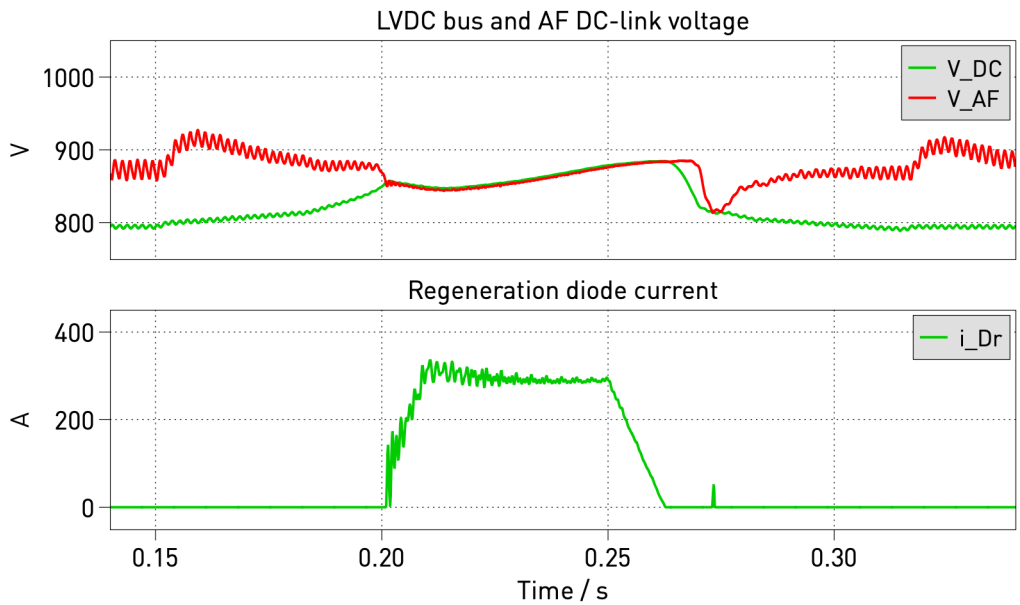


Fig. 9: DC bus voltage, AF DC-link voltage and regeneration diode current during the reverse power flow

3.2 Real-Time Simulation

For the real-time simulation, the analog and digital signals are looped back on the front panel of the RT Box as shown in Fig. 10. Tab. 4 lists the channels from the initialization commands.

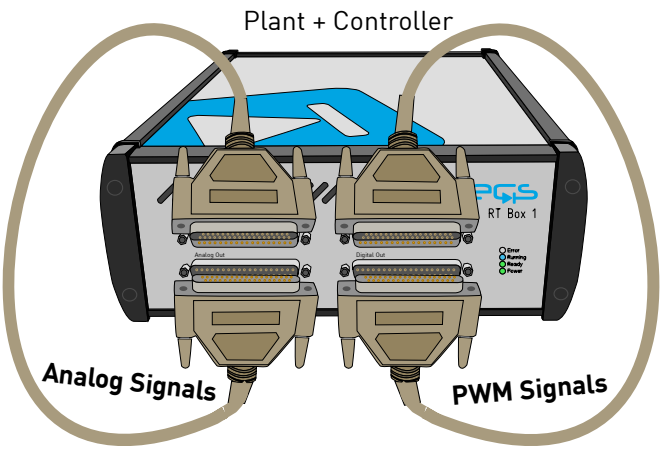


Fig. 10: Loop-back of the analog and digital signals on the front panel of a single RT Box

Table 4: Analog and digital I/O channels of the loop-back setup

Signal	Output	Input	Value at 10 V
MV phase voltages at the PCC	AO 0, 1, 2	AI 0, 1, 2	16 kV
AF converter currents	AO 3, 4, 5	AI 3, 4, 5	1,200 A
Input currents of "Rectifier Y"	AO 6, 7, 8	AI 6, 7, 8	2,000 A
Input currents of "Rectifier D"	AO 9, 10, 11	AI 9, 10, 11	2,000 A
AF DC-link voltage	AO 12	AI 12	1,200 V
DC load current	AO 13	AI 13	2,000 A
DC bus voltage (monitor)	AO 14	–	1,200 V
Regeneration diode current (monitor)	AO 15	–	1,000 A
Gate signals a+, a-, b+, b-, c+, c-	DO 0 to 5	DI 0 to 5	–

Please follow the instructions below to run the model on a single RT Box 2, 3 or 4:

1. Connect the analog outputs to the analog inputs and the digital outputs to the digital inputs with two 37-pin D-Sub cables, using the connectors that carry the channels of Tab. 4.
2. Open **Coder > Coder options...** and select the subsystem "Plant + Controller". In the **Target** tab, select your RT Box model as target and your RT Box as **Target device**. Keep the **Analog input voltage range** and the **Analog output voltage range** at ± 10 V, since the scaling of the Analog In and Analog Out blocks assumes this range.
3. Click **Build** to generate the code and upload the model to the RT Box.
4. In the **External Mode** tab, click **Connect** and then **Activate autotriggering**.

The scopes in the subsystem "Plant + Controller" now show the real-time data. The External Mode settings stored in the model record 8,000 samples with a decimation of 10, i.e. a time span of 0.4 s. In real time, the AF is enabled 50 ms after the start of the model, and the load profile repeats every 0.5 s. The Manual Signal Switch "AF switch" turns the AF off and on. With the AF off, the rectifier operates as a

passive 12-pulse rectifier, but the backfeed of the repeating load profile then charges the DC bus capacitors beyond the range of the analog outputs, as described above.

4 Conclusion

This RT Box demo model shows a hybrid MVAC-LVDC transformer for datacenters: a $1\,\mathrm{MW}$ 12-pulse diode rectifier that supplies an $800\,\mathrm{V}$ DC bus and an active filter that is connected to a third winding of the low-frequency transformer. The active filter reduces the THD of the grid current from $6.7\,\%$ to $1.4\,\%$, compensates the reactive power of $27\,\%$ of the active power, and, via the regeneration diode, returns power from the DC bus to the grid. The model is set up for real-time simulation on a single RT Box 2, 3 or 4: the electrical circuit with its diodes and the sub-cycle average converter runs on the FlexArray solver, and the controller runs in a second task on another CPU core, synchronized with the switching frequency. Offline, the same model emulates the loop-back connections and the controller latency. This allows the controller to be verified using a variable-step solver before its generated C-code implementation is tested under fixed-step, real-time execution conditions on the RT Box.

5 Bibliography

[1] J. Huber, P. Wallmeier, R. Pieper, F. Schafmeister, and J. W. Kolar, "Comparative Evaluation of MVAC-LVDC SST and Hybrid Transformer Concepts for Future Datacenters," in *Proceedings of the International Power Electronics Conference (IPEC 2022 - ECCE Asia)*, Himeji, Japan, May 2022.

[2] C.-C. Hou and C.-H. Tsai, "Design of an Auxiliary Converter for 12-Pulse Diode Rectifiers," in *Proceedings of the 3rd IEEE International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, Kaohsiung, Taiwan, June 2017, pp. 231-235. Click to access online: IEEE Xplore webpage[7].

[7] https://doi.org/10.1109/IFEEC.2017.7992042

Revision History:

RT Box TSP 4.1.1	First Release

How to Contact Plexim:

☎	+41 44 533 51 00	Phone
	+41 44 533 51 01	Fax
✉	Plexim GmbH Technoparkstrasse 1 8005 Zurich Switzerland	Mail
@	`info@plexim.com`	Email
	`https://www.plexim.com`	Web

RT Box Demo Model

© 2002–2026 by Plexim GmbH

The software PLECS described in this document is furnished under a license agreement. The software may be used or copied only under the terms of the license agreement. No part of this manual may be photocopied or reproduced in any form without prior written consent from Plexim GmbH.

PLECS is a registered trademark of Plexim GmbH. MATLAB, Simulink and Simulink Coder are registered trademarks of The MathWorks, Inc. Other product or brand names are trademarks or registered trademarks of their respective holders.