

RT Box

DEMO MODEL

SPI Interface Demo on a Single RT Box

Last updated in RT Box Target Support Package 3.1.2

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1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial communication interface specification used for short-distance communication, primarily with peripheral devices. SPI devices communicate in full duplex mode using a master-slave architecture between a single controller and multiple peripherals.

The SPI Controller and SPI Peripheral block from the RT Box Target Support Package implement SPI communication via digital outputs/inputs. There are 2 SPI modules available on the RT Box. Each SPI module can output data on up to 4 paralleled data channels (using a common clock and chip select signal).

This demo model shows:

- a demo scenario that wires the SPI Controller digital output channel with the SPI Peripheral digital input channel, as well as the SPI Peripheral digital output channel with the SPI Controller digital input channel,
- how to configure the parameters inside the SPI Controller and the SPI Peripheral block,
- SPI transmission within a single or multiple RT Box model steps.

One additional model shows the use case of the RT Box as SPI Controller connected to an external ADC device as the SPI Peripheral. This additional model is explained in the Appendix, and is part of the demo model folder.

1.1 Requirements

- One PLECS RT Box[1] and one PLECS Coder[2] license.
- The RT Box Target Support Package[3] (minimum version 2.2.1).
- Follow the step-by-step instructions on configuring PLECS and the RT Box in the Quick Start guide of the RT Box User Manual[4].
- Wire the Digital Output channel 0, 1, 2, 3, 4 respectively to the Digital Input channel 0, 1, 2, 3, 4 on the front pannel of the RT Box.

2 Model

This demo model uses one module as SPI Controller, and the other module as SPI Peripheral on the same RT Box.

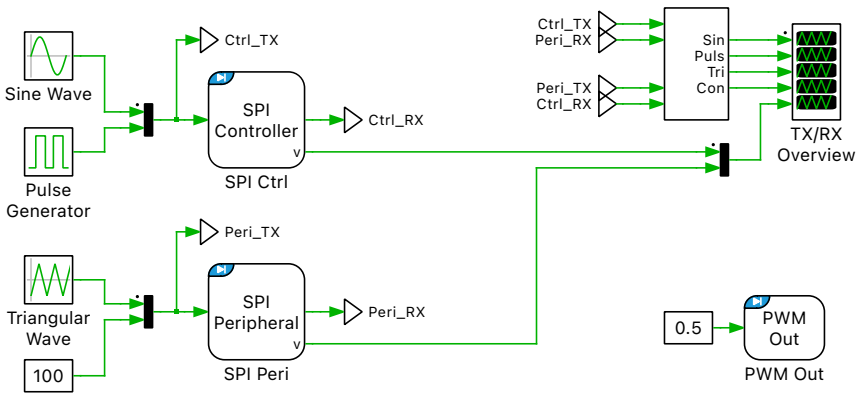


Fig. 1: Subsystem circuit schematic for the SPI Controller-Peripheral demo

[1] https://www.plexim.com/products/rt_box
[2] https://www.plexim.com/products/plecs/plecs/plecs_coder
[3] https://plexim.com/download/rt_box
[4] https://www.plexim.com/sites/default/files/rtboxmanual.pdf

The circuit schematic is shown in Fig. 1. A Sine wave and a Pulse wave are packed into two 16-bit words and transmitted out from the SPI Controller data output channel. With the hardware wiring, it is received at the SPI Peripheral data input channel. Likewise, a triangular wave and a constant value are transmitted from the SPI Peripheral data output channel to the SPI Controller data input channel. Both the transmitted original signals and the received signals are displayed in the Scope in Fig. 1 for comparison.

Additionally, a PWM Out block generates a PWM signal with 0.5 duty cycle synchronized with the RT Box model step size by configuring its **Synchronization with model step** option as `Enabled`. This PWM signal can be used as a reference to observe the different behaviors of SPI transmission within a single or multiple RT Box model steps.

Fig. 2 shows the mask content of the SPI Controller block. For the fields not mentioned in the following explanation, please refer to the **Help** page of the SPI Controller block.

2.1 SPI Controller Setup tab

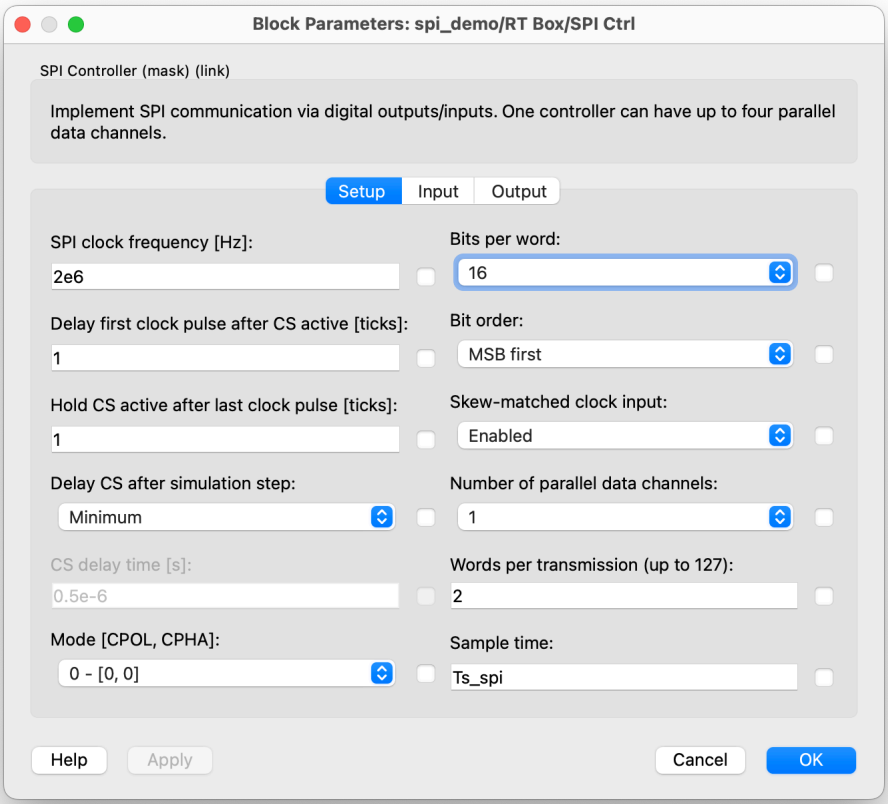


Fig. 2: Mask content of the SPI Controller block

- The **Delay first clock after CS active** and **Hold CS active after last clock pulse** fields are used in case of special timing needed between the clock signal and CS (chip select) signal. In this demo the default value of 1 (tick) is used in each field.
- The **Delay CS after simulation step** is useful to adjust the beginning of SPI data transmission with regards to the RT Box simulation step. In this demo, `Minimum` is used by default.
- **Mode [CPOL, CPHA]**: Note that the same SPI mode has to be configured between the SPI Controller and an external SPI Peripheral device to ensure correct data interpretation.

- **Skew-matched clock input** can be enabled when the signal transmission delay from the controller output to its input exceeds half an SPI clock period. When enabled, the corresponding **Digital input channel for skew-matched SPI clock** under **Input** tab has to be specified to receive the incoming clock, otherwise this field is greyed out.
- **Number of parallel data channels**: Note that the dimension of the **Digital input channel(s) for SPI data** and **Digital output channel(s) for SPI data** under **Input** and **Output** tabs has to match the number chosen here. In this demo only 1 data channel is used.
- **Words per transmission**: In this demo, one word is used for the Sine wave and the other word is used for the Pulse wave.
- **Sample time**: Putting `0` here means that the SPI transmission happens within every single model step. The SPI transmission can also be extended over multiple model steps by putting a number here which is an integer multiple of the model step size. In the following section, it showcases both scenarios. Besides, putting `-1` means to inherit the sample time of the Atomic Subsystem or Task frame that this SPI Controller block resides in.

2.2 SPI Controller Input and Output Tabs

Since each SPI module can only output one SPI clock signal and one CS signal, the **Digital output channel for SPI clock** and **Digital output channel for CS** require both a single channel number.

2.3 SPI Peripheral

The mask content of the SPI Peripheral block is the same as that of the SPI Controller, except for several CS (Chip Selection) timing related fields. Thus it is not discussed again.

3 Simulation

From the **System** tab of the **Coder options...** window, select the "spi_demo/RT Box" Subsystem and go to the **Target** tab. **Build** the "RT Box" model onto the RT Box. Once the model is uploaded, from the **External Mode** tab of the **Coder options...** window, **Connect** to the RT Box and **Activate autotriggering**. The real-time simulation results can be observed via PLECS Scope called "TX/RX Overview". One can also change the Constant with value of 100 into, for example 200, and observe the immediate change in the received value.

3.1 SPI Transmission within a Single Model Step

This is the default setup in the Model initialization commands of this demo model. It is done by enabling `type = 'single'`, which sets:

- RT Box discretization step size = $20\,\mu$s
- SPI transmission sample time = $20\,\mu$s

Once the real-time simulation is running on the RT Box and the external mode is enabled, the waveforms in the scopes are recorded. The most important waveforms in "TX/RX Overview" Scope are shown in Fig. 3. The received values match their transmitted original values in terms of signal amplitude and frequency. This validates the SPI Controller-Peripheral functionality on the RT Box.

Fig. 4 on p. 6 shows the zoom-in of Fig. 3 around $0.3\,$s. The incoming SPI Controller data exhibit a staircase waveform with step size of $20\,\mu$s, which equals to the RT Box discretization step size. There is a delay of two SPI transmission intervals between the outgoing reference signal and the received data.

For more insight on the timing, an external oscilloscope is used to measure the different digital channels and the RT Box step size. In Fig. 5 on p. 7 probe CH1 shows the 0.5 duty cycle PWM synchronized to the $20\,\mu$s model step size. Since the PWM is generated with positive polarity, from the center of the high state to the center of the next high state marks exactly one model step. One can see that in this scenario, the SPI transmission happens within every RT Box model step. Note that due to limited number of channels on the oscilloscope, only the Controller output (SIMO) data bus is probed in Fig. 5 on p. 7 and the Peripheral output (SOMI) data is not measured.

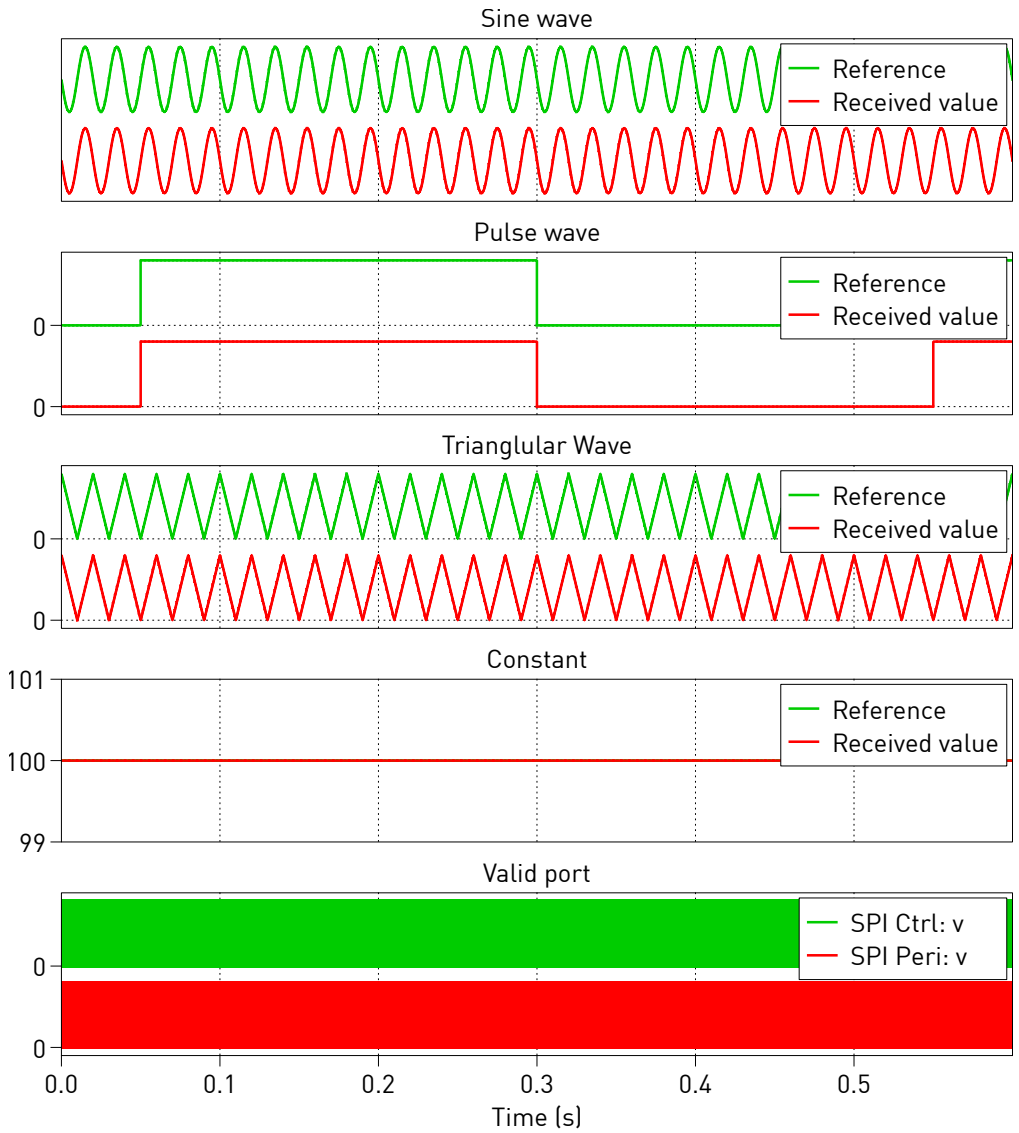


Fig. 3: Real-time simulation result on PLECS Scope for SPI transmission within a single model step

3.2 SPI Transmission over Multiple Model Steps

This scenario can be chosen by commenting out the previous `type = 'single'` and enabling `type = 'multi'` in the model initialization commands of this demo model. This sets:

- RT Box discretization step size = $5\,\mu s$
- SPI transmission sample time = $20\,\mu s$

This is to demonstrate the case when the SPI transmission time (approx. SPI clock period x Bits per word x Words per transmission) requires more time than what a single RT Box step offers. Note that the SPI transmission interval can only be integer multiples of the RT Box step size.

The real-time simulation waveforms on the "TX/RX Overview" Scope look similar to Fig. 3 on a large time scale. However, the zoom-in shown in Fig. 6 on p. 8 reveals the difference. For example, the Sine wave reference signal is discretized with $5\,\mu s$ now, while the incoming SPI data is still updated every $20\,\mu s$. The complete SPI transmission takes 4 full RT Box calculation steps. There are still two SPI transmission steps delay in the loop-back scenario between the reference signal and the received data.

Fig. 7 on p. 8 provides more insight with the oscilloscope measurement. Probe CH1 shows the 0.5 duty cycle PWM indicating the new $5\,\mu s$ model step size. CH2 to CH4 show the SPI transmission at $20\,\mu s$

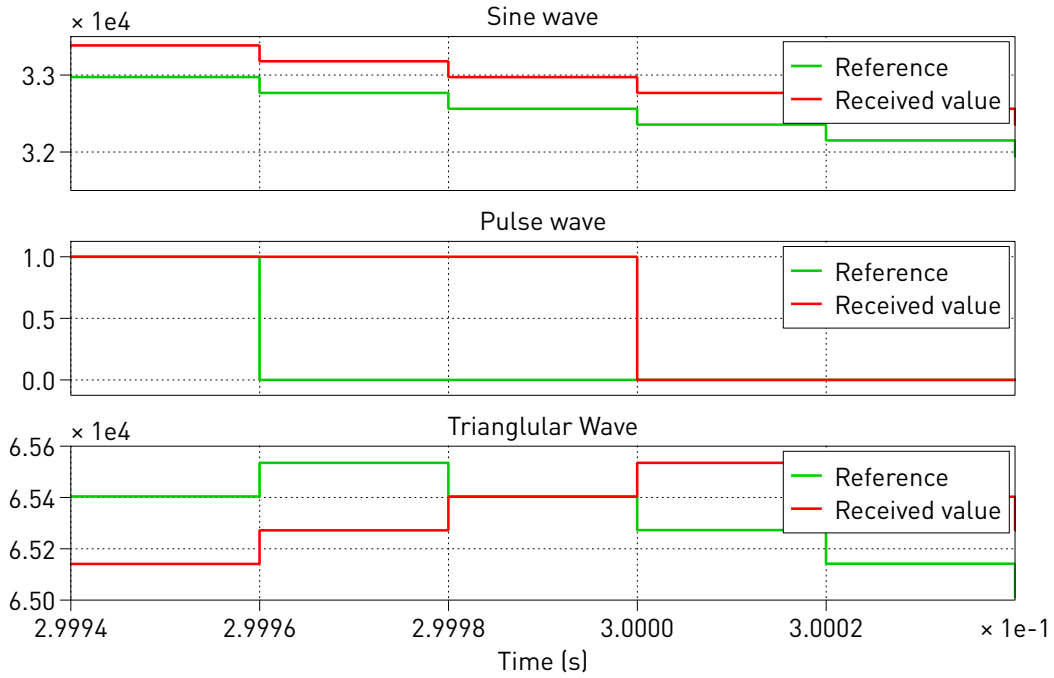


Fig. 4: Zoom-in around 0.3 s of the real-time simulation result on PLECS Scope for SPI transmission within a single model step

sample time, which are exactly 4 times a model step.

4 Conclusion

This RT Box demo model demonstrates a Controller-Peripheral test using the integrated SPI interface on the RT Box. It shows how to set up the SPI Controller and Peripheral blocks in a PLECS model. The demo model runs in both offline and in real-time simulation.

5 Appendix

For the "SPI Transmission within a Single Model Step" case, a more advanced demo model, named `spi_demo_adc`, is available in the demo model folder. Running this demo requires an external ADC evaluation board, specifically the **EVAL-AD7980-PMDZ** from Analog Devices. The user guide for the evaluation board is provided in [2]. The pinout of the evaluation board is shown in Fig. 8 on p. 9 and the connection to the RT Box is depicted in Fig. 9 on p. 9.

The RT Box functions as the SPI controller, receiving SPI data from the external ADC board. It also generates a sinusoidal analog signal between 0.5 V and 4.5 V at 50 Hz. The 16-bit ADC evaluation board (EVAL-AD7980-PMDZ) converts this analog signal into digital values and acts as the SPI peripheral, sending the converted data to the RT Box SPI interface.

Note that in this demo the RT Box SPI CS signal is used as the CNV (conversion start) signal of the ADC and the ADC SDI pin is tied up to the supply voltage. Please see section "3-WIRE CS MODE WITHOUT BUSY INDICATOR" in [1]. In case of using two AD7980 devices together, one might need specific timing patterns of CNV, and CS1 CS2 for SDI pin of each ADC. In this case, duty cycle and carrier phase shift of the PWMs synchronized with the SPI transmission sample time can be properly adjusted to achieve the desired signals.

The RT Box subsystem circuit schematic is shown in Fig. 10 on p. 9. Scope "Ref/RX Overview" shows the comparison between the analog reference signal sent out from the RT Box and received SPI data after external ADC conversion.

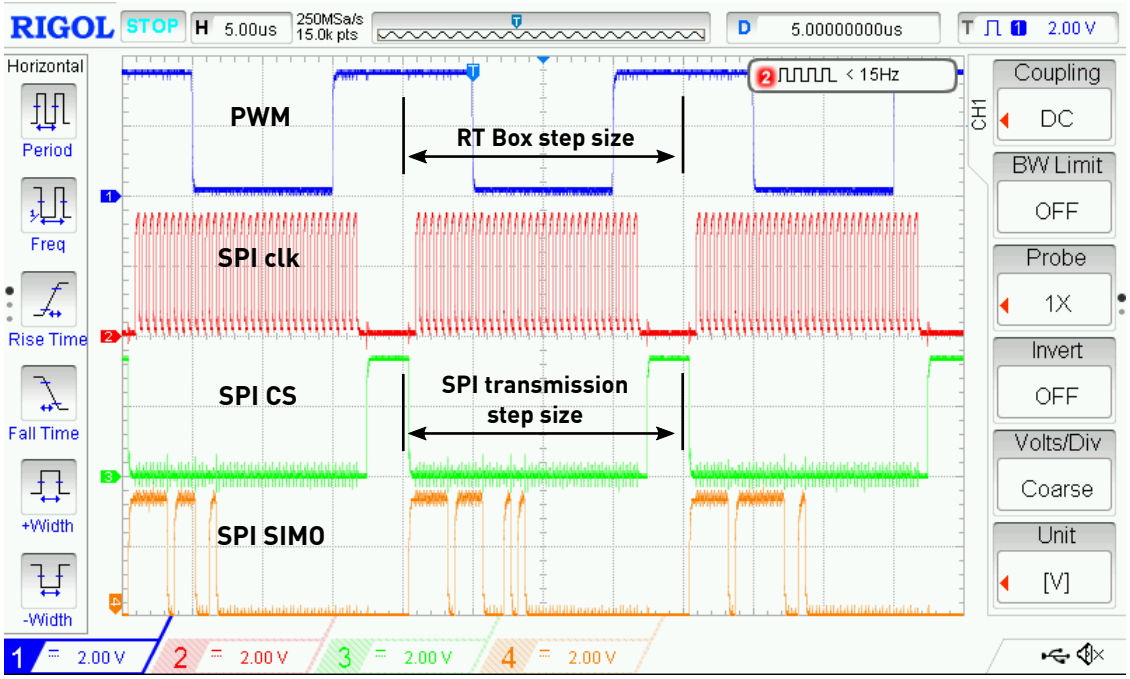


Fig. 5: External oscilloscope measurement for SPI transmission within a single model step

Once the model is uploaded onto the RT Box and the external mode is enabled, the real-time simulation results can be observed as shown in Fig. 11 on p. 10.

6 Bibliography

[1] Analog Devices AD7980 datasheet [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/AD7980.pdf.

[2] Analog Devices EVAL-AD7980-PMDZ user guide [Online]. Available: https://www.analog.com/en/resources/evaluation-hardware-and-software/evaluation-boards-kits/eval-ad7980-pmdz.html.

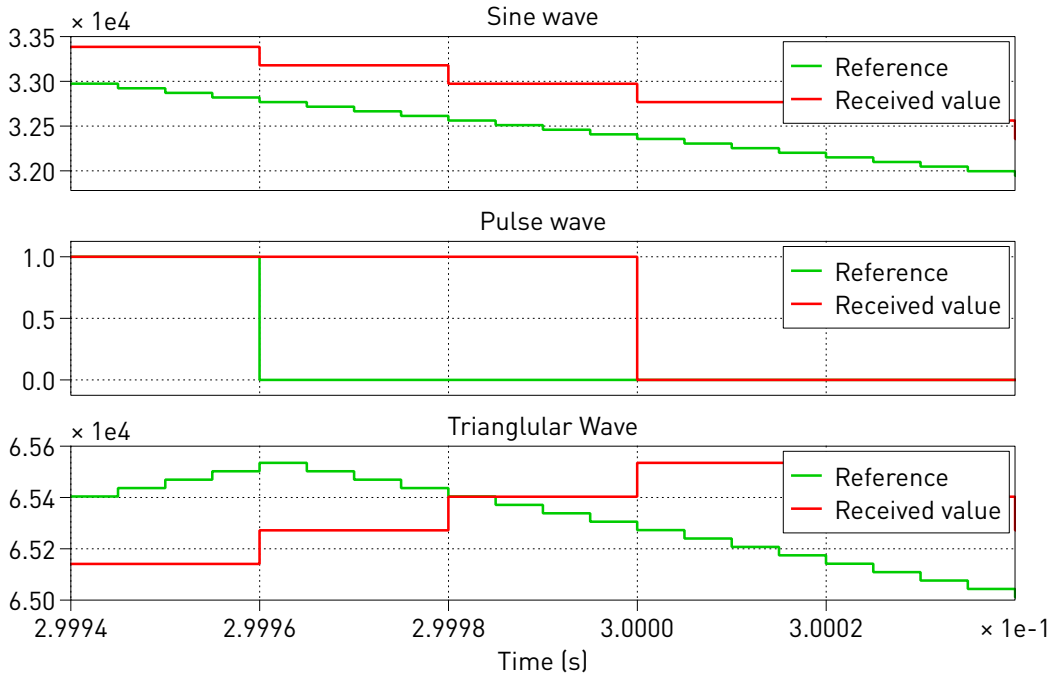


Fig. 6: Zoom-in around 0.3 s of the real-time simulation result on PLECS Scope for SPI transmission over multiple model steps

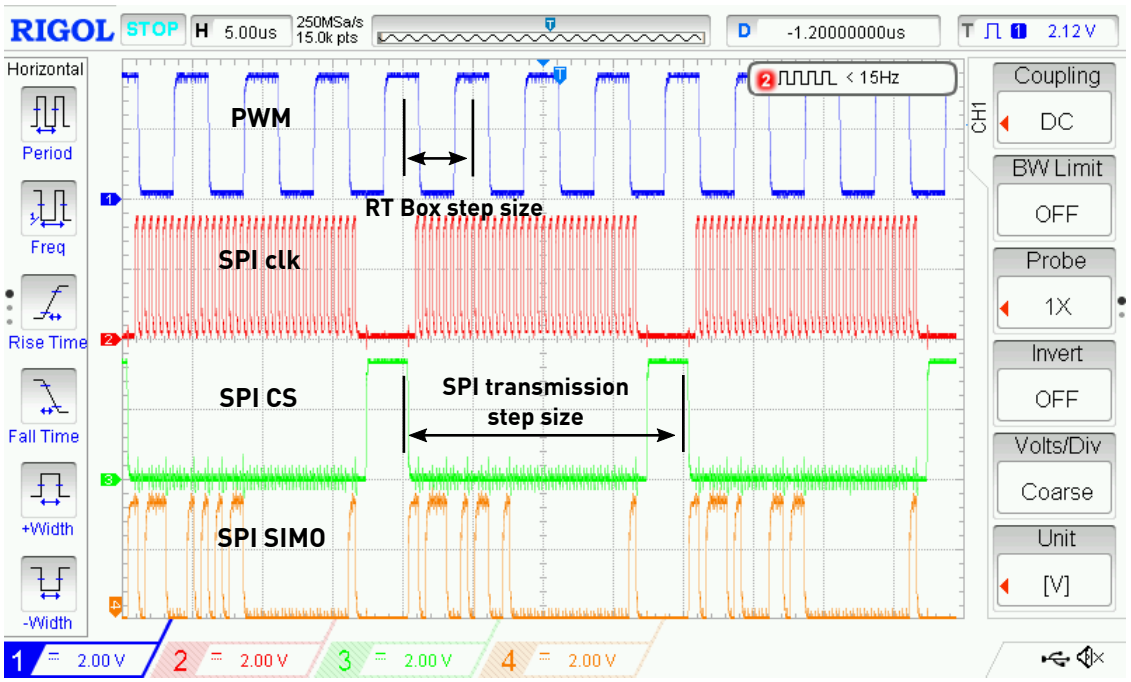
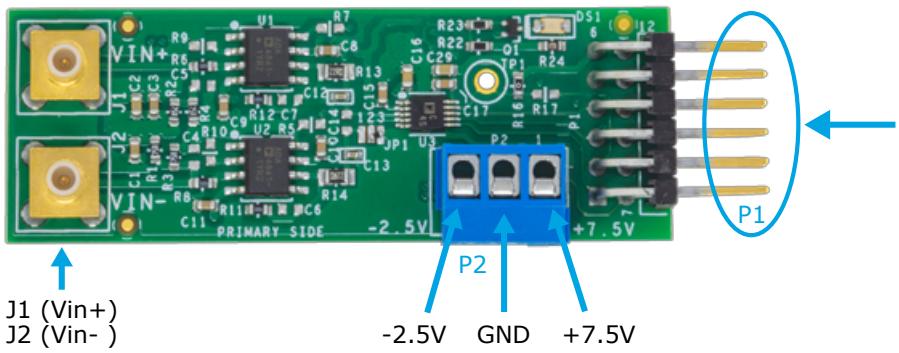


Fig. 7: External oscilloscope measurement for SPI transmission over multiple model steps



Pin	Function	Pin	Function
1	CNV (CS)	7	NC
2	NC	8	NC
3	MISO	9	NC
4	SCLK	10	NC
5	GND	11	GND
6	VCC	12	VCC

Fig. 8: ADC Evaluation Board used as SPI peripheral with Pinout description

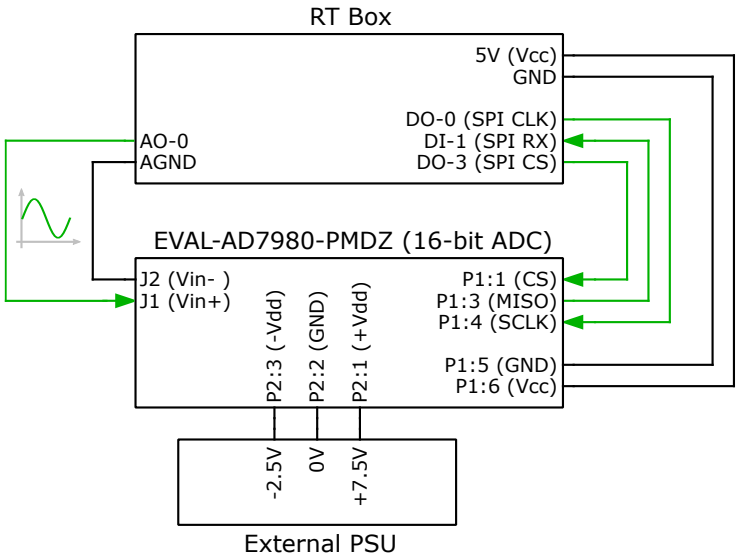


Fig. 9: Pin connection between the RT Box and the external ADC board for the advanced SPI demo

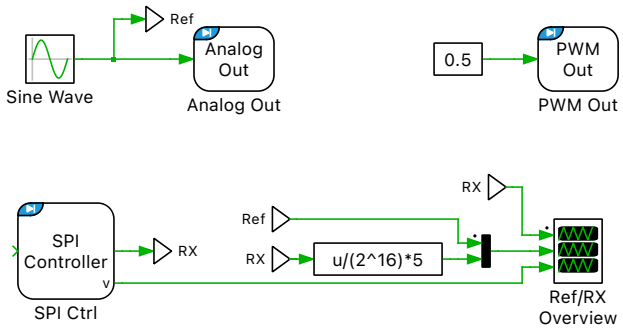


Fig. 10: Subsystem circuit schematic for the advanced SPI demo on the RT Box

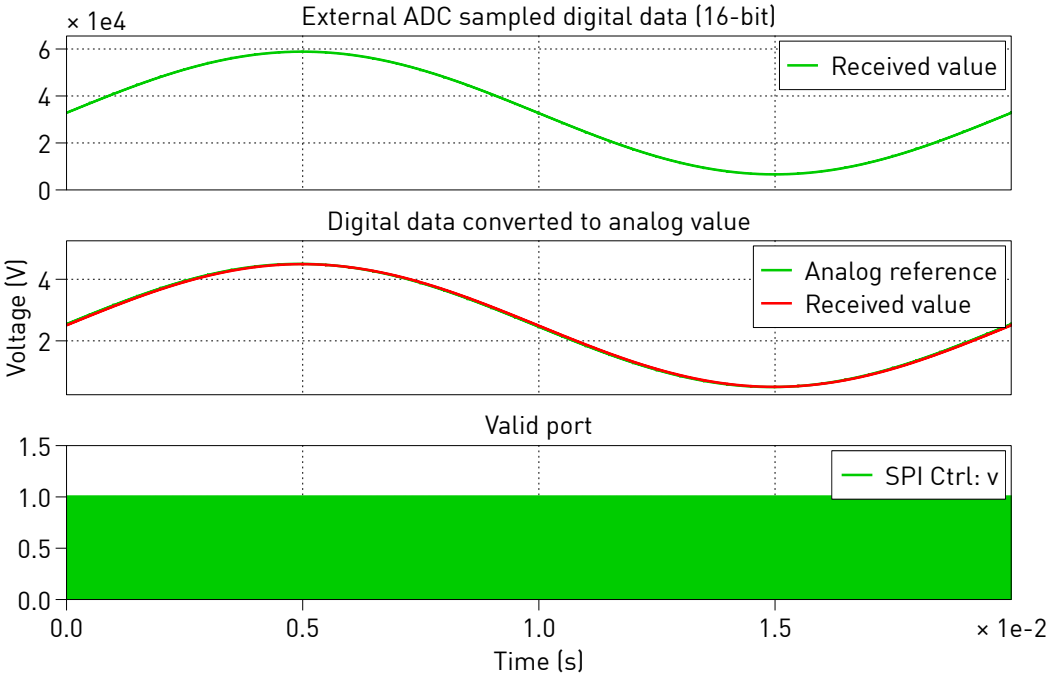


Fig. 11: Real-time simulation result on PLECS Scope of the advanced SPI demo

Revision History:

RT Box TSP 2.1.1	First release
RT Box TSP 2.2.1	Include SPI Slave
RT Box TSP 3.1.2	Update to use the Controller-Peripheral terminology

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RT Box Demo Model

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